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December 1995

TRANSFER OF OPTICAL PROCESSING TO SYSTEMS (TOPS): PHASE-ONLY CORRELATOR

Martin-Marietta Technologies, Inc.

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TRANSFER OF OPTICAL PROCESSING TO SYSTEMS (TOPS): PHASE-ONLY CORRELATOR

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13. ABSTRACT (Maximum 200 words)

This report contains the details of the effort performed in the conduct of the TOPS program. These details include descriptions and performance evaluations of the various pattern recognition algorithms used in the final demonstrations. The report contains a description of the delivered optical processor hardware (SPOTR) and details of the tower and captive carry flight testing.

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Foreword

This document is prepared for the Electronic Systems Division, Air Force Systems Command under Contract F19628-91-C-0155 and is submitted in accordance with Exhibit A, CDRL Sequence Number A002.

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The approach used in the creation of the Final Report is to define and summarize the final status of the key elements of the TOPS program. A description of the algorithms and hardware used and the final testing performance will be provided. A chronological history of the program will not be provided.

Three additional portions of this report (which are not published here) include the User's Manual, Interface Control Document, and Optical Subsystem Alignment Procedure. Copies of these portions may be obtained from RL/EROP, Hanscom AFB MA 01731.

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1.0 Executive Summary

The Martin Marietta TOPS Optical Pattern Recognition program is sponsored by the Advanced Research Project Agency (ARPA) under the direction of Brian Hendrickson and Dr. Andrew Yang. The program is managed by Rome Laboratory, Hanscom AFB under the direction of Dr. Joe Horner. End user support for the program is provided by the U.S. Army Missile Command (MICOM) Research, Development, and Engineering Center and the Non-Line of Sight (NLOS) program office. The team members working on this project include the University of Dayton Research Institute, Boulder Nonlinear Systems, U.S. Army MICOM and Martin Marietta.

1.1 Objective

The Martin Marietta TOPS program has two objectives; to develop and demonstrate the performance of an autonomous optical pattern recognition system and to transition the optical pattern recognition technology to existing and future systems. The fiber optic guided missile (FOG-M) mission was chosen as the application focus to demonstrate real time target acquisition assistance to the missile gunner. The purpose of the optical correlator is to provide target overlay symbology on the FOG-M video monitor and to be available to provide tracking data to a digital tracker. Finally, the optical processor can be used to assist in the identification of friend or foe by discriminating between the target of interest and other vehicles via the shape of the target. The performance of the optical correlator system is designed to comply with the derived target recognition requirements of the FOG-M while complying with the derived physical and environmental requirements of the helicopter used to simulate the missile flight.

1.2 Approach

The Martin Marietta TOPS Optical Pattern Recognition program is divided into three phases; a Development Phase, a Prototype Phase and a Demonstration Phase. During the first two phases of the TOPS program a concurrent Martin Marietta funded capital equipment program, Systems Development, supported TOPS in the building of three optical correlator systems. The general approach philosophy involves the development of a real time system taking advantage of the strengths of both digital electronic and optical processing in a compact and rugged package capable of a variety of testing applications with only minor software modifications.

The major TOPS tasks of the Development Phase are a FOG-M mission requirements analysis, a mission requirements definition and an optical processor system design. During the Development Phase the Systems Development program developed two compact optical correlators based on magneto-optic and ferroelectric liquid crystal spatial light modulators (SLMs). The purposes of this activity is to evaluate and down select to one of the two SLM technologies and develop the skills necessary to fabricate compact correlators. Pattern recognition algorithms (preprocessing and filtering) are also developed and evaluated during the Development Phase.

The major TOPS tasks of the Prototype Phase are the preliminary design of the delivered System for Passive Optical Target Recognition (SPOTR) and support for the fabrication and performance validation of a SPOTR prototype called the Flyable Prototype optical processor. The Martin Marietta Systems Development program provided the material and a majority of the labor to support the design and fabrication of the Flyable Prototype which complies with the TOPS performance, physical, and environmental requirements. Pattern recognition algorithms continued to be developed (postprocessing, filter management and controller software) and enhanced during the Prototype Phase.

The Demonstration Phase tasks include the fabrication, delivery and demonstration of the deliverable SPOTR. These tasks resulted in a demonstration program at US Army Missile Command (MICOM). The demonstration program involves recognizing and locating M60A2 tanks and providing a recorded video and text file of the processed SPOTR performance while sitting atop a 300 foot tower and while flying helicopter flight profiles consistent with a FOG-M mission.

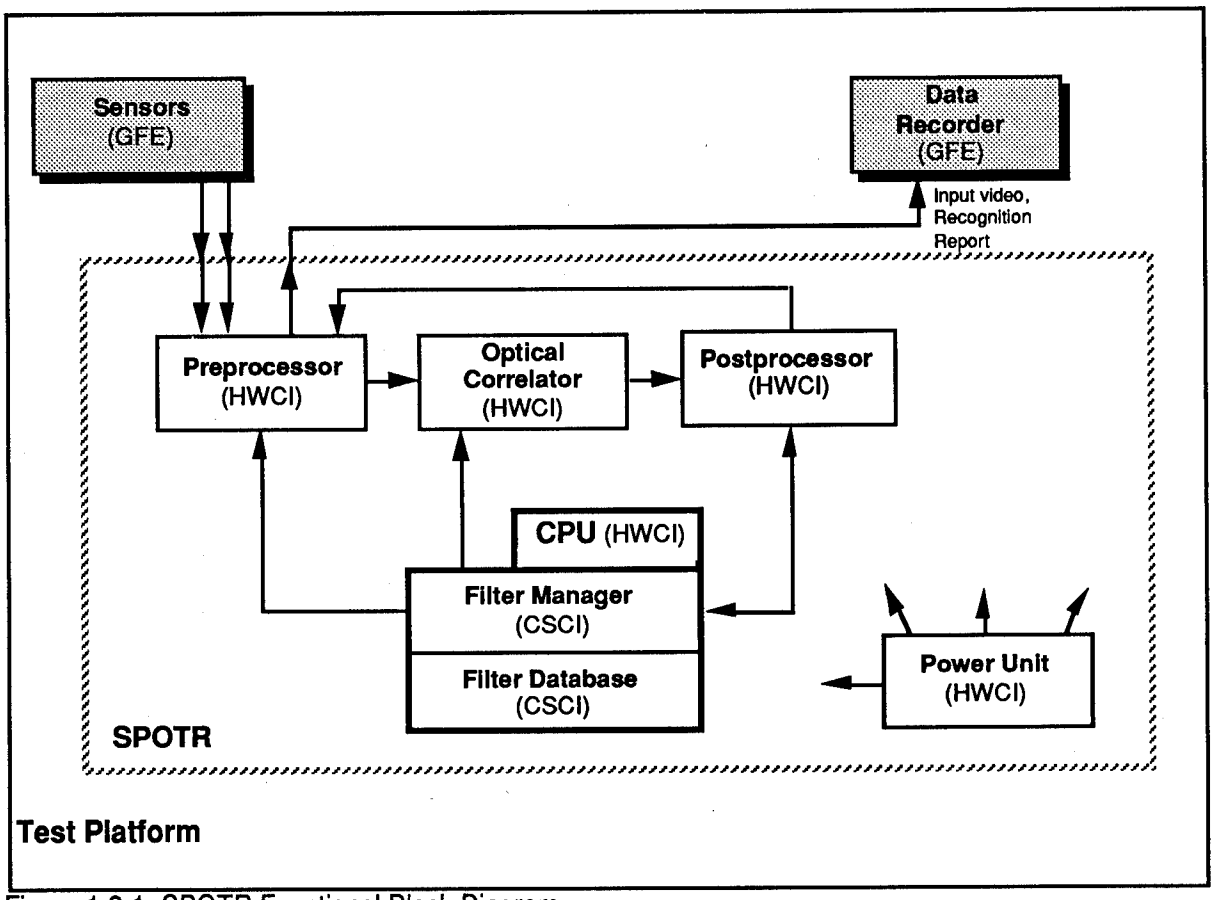


Figure 1.2-1 SPOTR Functional Block Diagram.

The approach taken for the design of the SPOTR and associated algorithms was to develop a real time, highly discriminatory processing system based on a hybrid of electronic and optical processing subsystems. The resulting SPOTR includes a variety of custom and commercial electronic processors which emphasizes algorithm and system control flexibility with state of the art throughput and packaging size and an optical co-processor which is optimal for the execution of the correlation function in a compact and low power consumption architecture. Figure 1.2-1 illustrates the functional block diagram of the SPOTR. The SPOTR accepts up to four RS-170 composite video input signals via the preprocessor. The preprocessor formats the imagery for insertion into the optical processor (correlator function). The optical correlator accepts the processed input and a pre-computed correlation filter chosen from a data base by the filter manager. The resulting correlation function is further processed by the postprocessor which makes a target detection and location determination based on certain qualities of the correlation plane data. Based on that determination a location is communicated to the preprocessor which outputs the incoming RS-170 composite video with target detection symbology overlay and also communicates with the filter manager to determine the next best set of filters to exercise in the correlator.

1.3 Technical Performance

A series of tests were conducted to evaluate the performance of the optical pattern recognition system. These tests were designed and implemented throughout the life cycle of the program to validate system designs and to measure functional and target acquisition/tracking performance in the field. Tests were conducted on the various components and subsystems of the processor to ensure compliance with allocated performance requirements and functionality. In turn system-level functional tests were conducted to assess full operational capability and to evaluate performance parameters such as optical quality, throughput, latency, location accuracy, power consumption, and weight. All components, assemblies, subsystems meet or exceed their allocated performance and physical requirements. Thus the SPOTR system meets or exceeds all of its design requirements.

To validate the processor design for the UH-1 helicopter environment the Flyable Prototype processor was developed under Martin Marietta funding. The "Flyable" was used to conduct thermal and acceleration tests prior to the SPOTR critical design review. The Flyable was successfully tested under operating conditions over 48°-110° F and under acceleration environments 6dB higher than the maximum expected value measured on the UH-1.

The field testing of the optical processor was conducted at Redstone Arsenal, AL in conjunction with the US Army Missile Command (MICOM). The Tower Test provided a controlled environment to establish a working test configuration with the visible missile seeker and data collection flight rack. In addition, the target acquisition and tracking algorithms were refined and evaluated with the use of the M60A2 tank as the target of interest and several other military targets. Algorithm studies conducted in the Tower Test included target aspect and background clutter sensitivity evaluations. The processor performance did not vary as a function of sensor depression angle relative to the target over the designed range. The processor showed some sensitivity as a function of target azimuth orientation relative to the sensor. It was found that broadside targets are easier to acquire than end-on orientations. This is consistent with the known Johnson Criteria which defines a direct relationship between target acquisition performance and the number of pixels defining the target in the image.

Flight testing provided the opportunity to evaluate and demonstrate the application of optical processing to visible missile seeker target acquisition and tracking. The flight testing consisted of flying missions consistent with typical Fiber Optic Guided Missile (FOG-M) profiles. These flights, "missions", were flown over ranges from 2 kilometers into 200m in which over 2000 384x384 frames of imagery were processed in approximately 120 seconds. In 20 missions analyzed the processor acquired and tracked the M60A2 tank 100% of the time at acquisition ranges in excess of 1.5 km. On any given frame of the 40,000 processed the probability of identifying the M60A2 target was on average 90%. The probability of falsely identifying another type of military vehicle as the M60A2 was 4%. These missions included battlefield scenarios which included discrimination of T-72 tanks and various armored personal carriers, targets conducting evasive maneuvers, the target having a 55 gallon drum added to its configuration and being placed about 10% into a densely forested tree line.

1.4 Summary

The TOPS Optical Pattern Recognition program was highly successful in meeting its technical and programmatic objectives. The optical processor proved to be very reliable in flight environments and demonstrated performance capabilities consistent with the requirements of many tactical anti-armor missile target acquisition and tracking systems. The program was completed within one week of the scheduled three year period of performance, was on cost and will deliver a state-of-the-art optical

processing system for future applications. In supporting the "Transfer" objective of TOPS, we have successfully transitioned the processor and algorithms to the US Army in support of The Army's Combined Arms Weapons System (TACAWS) and the US Air Force in support the Optical Processor Enhanced LADAR program.

2.0 Preprocessing

The objective of this task is to develop an interface between the sensor and the optical processor. In addition, to provide the electrical and mechanical connections, this interface is tasked with operating on the sensor data to enhance the optical processor pattern recognition performance and provide a visual output of the processor performance. The challenge associated with this task is that there is a mismatch in the array sizes or space-bandwidth product (SBWP) between the sensor and the processor and there is also a mismatch in the number of available modulation states (gray scale levels) between the seeker imagery and the spatial light modulators SLM. The seeker used in TOPS provided a SBWP of 512x480 with 8 bits of gray scale. The ferroelectric liquid crystal (FLC) SLMs used in the TOPS program have SBWPs of 128x128 and 1 bit of gray scale modulation. Due to these mismatches a preprocessing algorithm must be used in order to condition the sensor imagery for insertion into the input SLM. In addition, it is desirable to process the sensor imagery prior to insertion into the correlator to enhance those features of the imagery which are conducive to improved correlation performance.

Because of the basic operation of the seeker used in the TOPS program and the limited stability of its mount and gimballing system the video imagery taken in the helicopter is blurred. The basic phenomena is a spatial displacement of the two video fields in the video frame. This displacement is due to a 1/60th of a second latency between fields which becomes significant when the sensor platform moves quickly. This phenomena differs from excessive exposure time for each field as the sensor shutter speed was approximately 1/10,000th of a second. The significance of this displacement is time dependent and ranges from none (registered fields) to several percent shift of one field with respect to the other. The impact to correlation performance can range from even slight peak energy improvements (very slight blur) to the generation of two correlation peaks caused by separated representations of the target in the two interlaced fields. Finally, the visible seeker used is limited in its ability to compensate for varying lighting conditions even as subtle as that caused by a single cloud casting a shadow over a portion of the field of view. This scenario causes widely varying video levels being presented to the SPOTR which, if not properly accounted for, can result in dramatic changes in the appearance of the raw and subsequently preprocessed image.

The general methodology we have chosen in TOPS for addressing the technical problems highlighted above implements the diff-3 operator which has been reportedly in early reports. Subsequent to coining the name diff-3 we learned that a very similar algorithm had been reported called the "range" operator. In doing so we have limited our choice in algorithms to that which can be implemented in real time by existing image processing hardware to minimize the cost of the preprocessing hardware development.

The processing algorithm starts when an incoming video image is grabbed and digitized with the Sharp GPB-1 NTSC image processing card. In the SPOTR we support both the 2° and 8° field of views from the sensor with independent inputs to the Sharp card. The Sharp GPB-1 NTSC image processor has been selected for the preprocessor hardware. With a combination of

hardware and software, the preprocessor first digitizes the image at 512x480 resolution and next subsamples every other line in the vertical to minimize the image blurring effects caused by the nonstabilized sensor platform described above. This 512x240 image is then windowed down to a 384x240 and then averaged and subsampled by 3 in the horizontal and by 2 in the vertical resulting in a 128x120 image. The image is centered on a 128x128 and passed to the diff-3 algorithm which is a 3x3 sliding kernel that outputs the difference between the maximum and the minimum pixels in the kernel. The histogram of this 'difference image' is then generated. A threshold is calculated using the histogram to ensure that 10% of the pixels will be in the 'on' state when the image is binarized. The 10% condition is an empirically derived number based on numerous studies involving the TOPS imagery. It is reasonable to assume that this number will vary with the sensor type. The percentage is adjustable during a mission in 0.5% increments with a keystroke on the user interface. This binary image is then interleaved in a format which is compatible with the SLM drive electronics. The 1-bit interleaved image is then transferred to the SLM electronics where it will be immediately written to the input SLM.

In addition, the analog-to-digital circuits on the SHARP board must also be initialized properly to insure that the grabbed images have a reasonable dynamic range. Artificial noise was believed to have been introduced into the SPOTR system as a result of low ambient light levels for the video sensor. The automatic gain and leveling circuitry in the seeker camera has been disabled, with the result that the output signal level varied significantly. The Sharp image processing board, which is used as the preprocessor in the SPOTR, has an ability to adjust the analog gain and level prior to digitization. However, at low light levels we believe the smaller dynamic range provided by the sensor was forcibly expanded, essentially performing a partial binarization of the image prior to performing the diff-3 (3x3 range) operation. In general, this led to poor correlation performance. To minimize the noise effect and maximize the sensor dynamic range, the SHARP board can be programmed to control the digitization dynamic range. A single frame is captured using the widest dynamic range available in the SHARP board and a histogram is then generated for this image. Two integrals are then tabulated, one starting at the bottom of the histogram (value of zero) and the other starting at the top of the histogram (value of 255). As soon as each integral reaches an empirically derived count of 0.05% of the total pixels in the image the process is halted. These two stopping points are then taken to be the lower and upper ends of the desired dynamic range and are programmed into the SHARP board accordingly.

The SPOTR preprocessing has worked as designed. It maximizes the useful dynamic range of the incoming analog video signal, it reduces the SBWP of the incoming 512x480 image to the necessary 128x128, it reduces the number of modulation levels from 256 to 2, it converts the image into a format usable by the SLM driver electronics, and displays the processed image with a cross-hair overlay all at a sustained 15 Hz rate. The diff-3 algorithm performed well as an edge enhancement utility pulling the target out of its background as long as the image provided by the sensor shows some difference in pixel values between the target and the background. On many occasions the only method of visually seeing the target array at Test Area 3 was to view the binarized image. At long ranges it is difficult to discern the shape of the M60A2 tank because of the large reduction in SBWP. In most instances the SPOTR was still able to perform well with the provided binary image. This is not a shortcoming of the preprocessing algorithm, but of the available SBWP in the input SLM. Non-target discrimination would be much more reliable if the SBWP of the input SLM could be increased, preferably to match that of the incoming video signal. This increase in SBWP would also force the issue of building a custom preprocessing board as the SHARP board would have more difficulty in sustaining the required throughput while performing the same functionality on a much larger number of pixels. For future programs it

would be highly desirable to build a custom preprocessing board which would perform all of the necessary tasks for converting the input image into data suitable for the input SLM. The custom board would be able to perform at much higher rates on much larger images and potentially better utilize the processing capabilities of an optical correlator.

Additional improvement in correlator performance might be gained by using SLMs that give 3 to 4 bits of modulation rather than the 1 bit of modulation that the SPOTR now has. Some preliminary simulations have shown that 3 to 4 bits of modulation can improve the correlation performance. This change would require the development of a new preprocessor to take advantage of the additional modulation levels. Additional information on the preprocessor is included in Section 5.0.

3.0 Spatial Filtering

Due to the wide range and multiple dimensions of possible target distortions in the TOPS demonstration program it is necessary to build "smart" filters which are capable of handling larger ranges of geometric distortions than a simple BPOF. Larger ranges of distortion invariance per filter are necessary in order to achieve real time target detection performance. While incorporating the geometric distortion invariance into the filter it is also important to maintain a discrimination capability as well as a uniform response across the distortion space of a filter to prevent unacceptable false alarm rates. In order to create these smart filters, reference imagery is necessary to provide spatial information about the target from all possible aspects.

The basic approach used to create the TOPS filters is to create a composite image using a number of references covering the distortion space desired in the smart filter. Weighted references are summed into a composite to create filters with improved invariance to geometric distortions of the target. Maintaining adequate discrimination is achieved by limiting the geometric distortion range covered by one filter in conjunction with the preprocessing algorithm used. The response uniformity of the filter across the designed distortion range is adjusted by the weighting of the references. The response uniformity is desirable to limit the required processor dynamic range and to ease the requirements of the postprocessing algorithm. This weighting is controlled using a variant of the Jared and Ennis (JE) algorithm.

The first step in developing the set of spatial filters is to determine the geometric distortion sensitivity of the M60A2 tank. The sensitivities were determined by finding the amount of distortion which generates a 3 dB reduction in peak energy from the auto-correlation peak. The differences in distortion values between the autocorrelation reference and the 3 dB down images are used to define the interval requirement built in a multi-reference (composite) filter. This interval is used to ensure adequate correlation performance across the entire distortion range.

The second step in developing the set of spatial filters for TOPS is to develop and test, in simulation and experimentation, various smart filters based on the distortion sensitivity information. From this we can develop the fine tuned design parameters and the spacing between smart filters and test them using our filter selection strategy. The efforts of the Martin Marietta independent research and development (IR&D) project D-22D prior to the beginning of TOPS have resulted in a robust algorithm known as the Improved Metric Sort (IMS) which is being used on TOPS. Separate and available documents describe the IMS formulation.

The third step in developing the set of spatial filters is to develop the complete set of filters necessary to perform the defined FOG-M captive carry mission. This involves extracting the reference images from the rest of the turntable data collection and developing the smart filters based on the knowledge learned in steps one and two. These steps are taken in several iterations as tradeoffs and modifications are made to the preprocessor, filters, and filter selection strategy.

The final TOPS filter set used in the SPOTR for the flight test at MICOM consisted of 810 composite filters covering a total distortion space of 360° azimuth, 6-12° elevation, -2° to 2° in-plane rotation, and cover target sizes over ranges from 1627 to 429 feet (range effectiveness was doubled by using two fields of view for the sensor, 2° and 8°) which allowed for 6500 to 429 ft mission coverage.

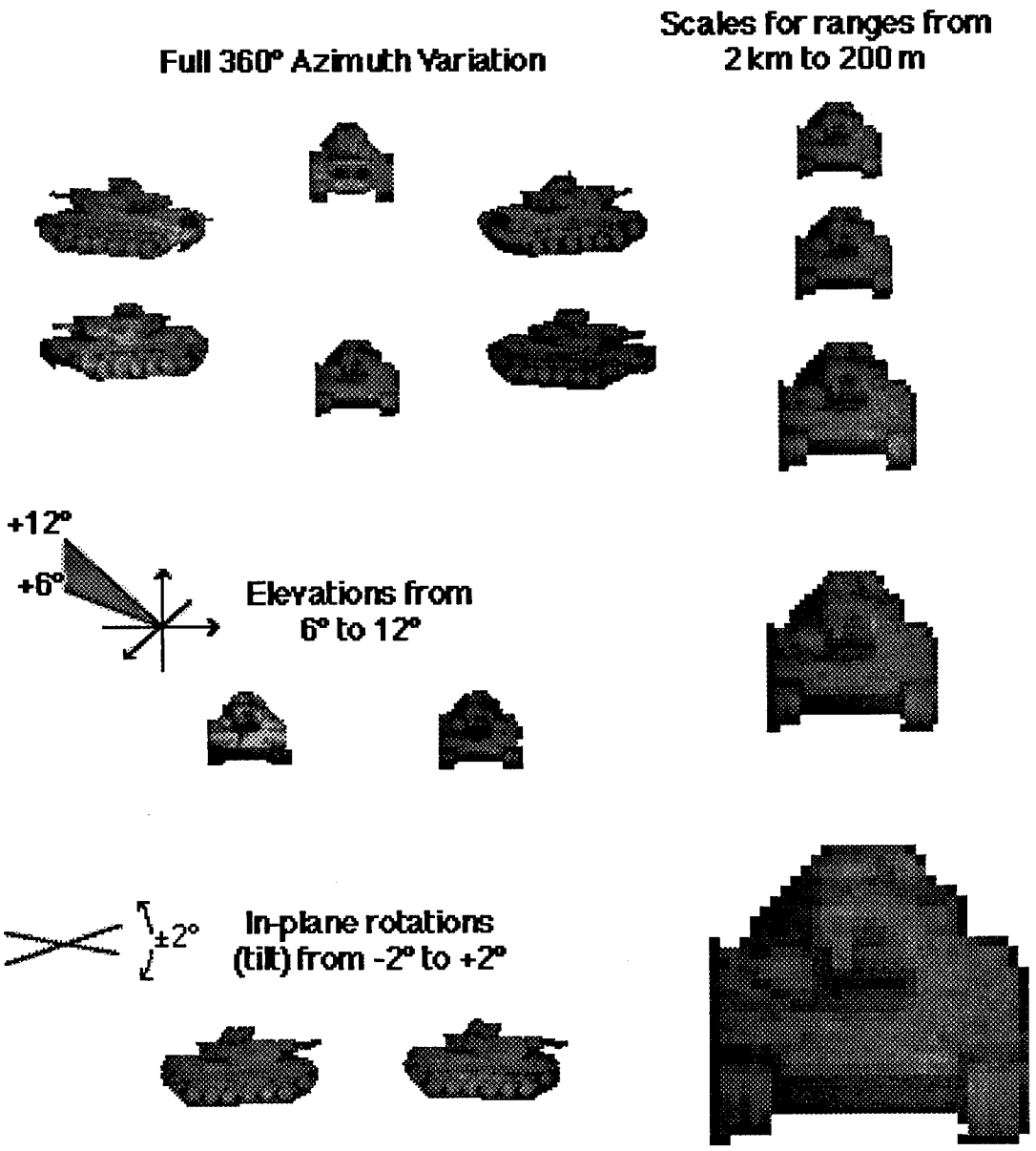


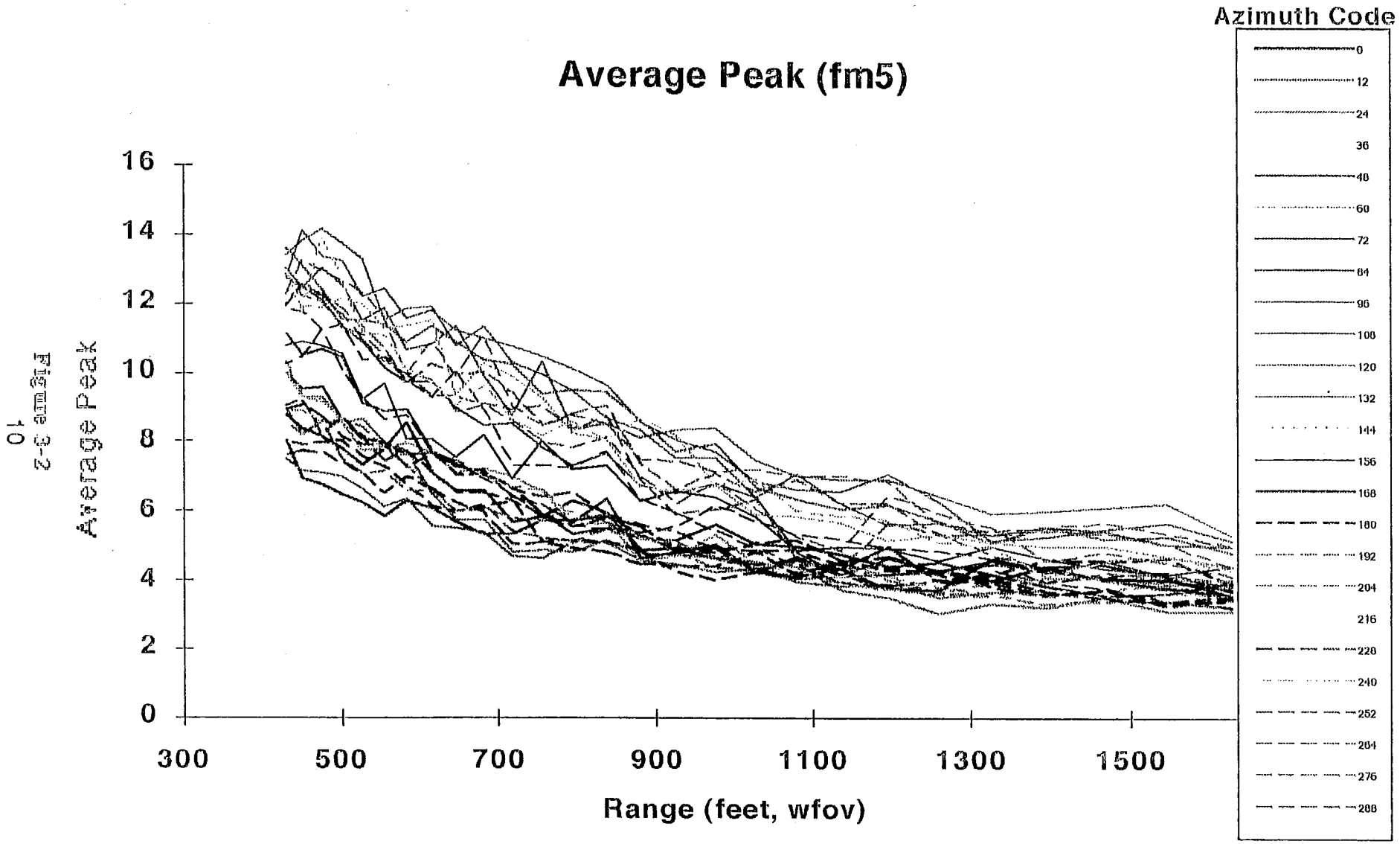
Figure 3-1 Turntable Reference Images.

All the TOPS filters were made from reference images collected from a M60A2 tank. The tank was mounted on a turntable which positioned the tank at various elevation and azimuth angles, enabling views of all aspects of the tank to be collected. These images were then used to fabricate the filters to be used in the flight tests. Reference images were electronically modified from the turntable imagery that was collected at MICOM. Since images were obtained for the various elevations and azimuths, only scale (range) and in-plane rotations needed to be computed. Digital interpolations of the images were performed to generate the appropriate magnification of the reference image for the desired ranges. The filter set used in the SPOTR for the tower and flight tests consisted of composite filters which were comprised of 5 scales per filter covering 5% of the nominal range. A similar interpolation was done for in-plane rotations of -2°, 0°, and 2°. These electronic manipulations were applied to grabbed images from 6°, 9°, and 12° elevation

angles and -3°, 0°, 3°, and 6° azimuth angles to generate a total of 180 reference images per composite filter. Figure 3-1 illustrates the distortions with reference images from the actual references used in the final filter set generation.

All the reference images were binarized using the preprocessing technique described in the Section 2.0, with the following modification. The binarization threshold was chosen for a 50% number of "on" pixels, excluding the zero value background pixels. This was done to increase the energy on target for improved correlations. The binarization level for 10% of the input scene pixels to be turned on gives a somewhat unpredictable number of pixels on target, and shading or lighting variations in the input imagery cause different edges to be turned on depending on environmental conditions. Since it is impossible to predict which edges will be extracted from the input scenes when field testing, the filter can be made more robust by allowing as many significant edges as possible to be extracted from the reference imagery. The 50% "on pixel" threshold results in allowing the most edges possible to contribute to the correlation signal which in turn results in a higher probability of detecting the target. The penalty paid for turning on more pixels in the reference image (50% vs ~10%) is that the correlation plane noise floor is likely to be raised; more "on" pixels in the reference image means more clutter is likely to be matched. This is a trade between probability of recognition and false alarm (more noise) rate. One solution to this problem is to develop a preprocessing technique that reduces or eliminates sensitivities to lighting variations, and is repeatable in results for reference images as well as real world images.

There are several characteristics which describe these correlation filters. The amount of energy on target (number of "on" pixels in a binary imagery which are describing the target) is proportional to the resulting correlation energy. The bigger the target (number of pixels with input energy), the larger the correlation peak. Azimuth variations (viewpoints around the target) have an effect on the number of pixels on target and therefore result in different correlation energy values. In terms of range, the farther away the target is the smaller its correlation peak will be for the same reasons. At the same time, the corresponding filter is more likely to respond to clutter in the scene since more matches will occur when the targets are less resolved and appear to look similar to each other. In other words, the noise floor rises while the correlation peak falls as a function of a number of these parameters which are all related to the number of pixels on target. Figures 3-2 and 3-3 illustrate the peak variations of the autocorrelations of the training set images (used in the composite filters) as functions of range (scale size) and azimuth.


Average Peak (fm5)
Average Peak
16
14
12
10
8
6
4
2
0
300
500
700
900
1100
1300
1500
Range (feet, wfov)
Azimuth Code
0
12
24
36
48
60
72
84
96
108
120
132
144
156
168
180
192
204
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240
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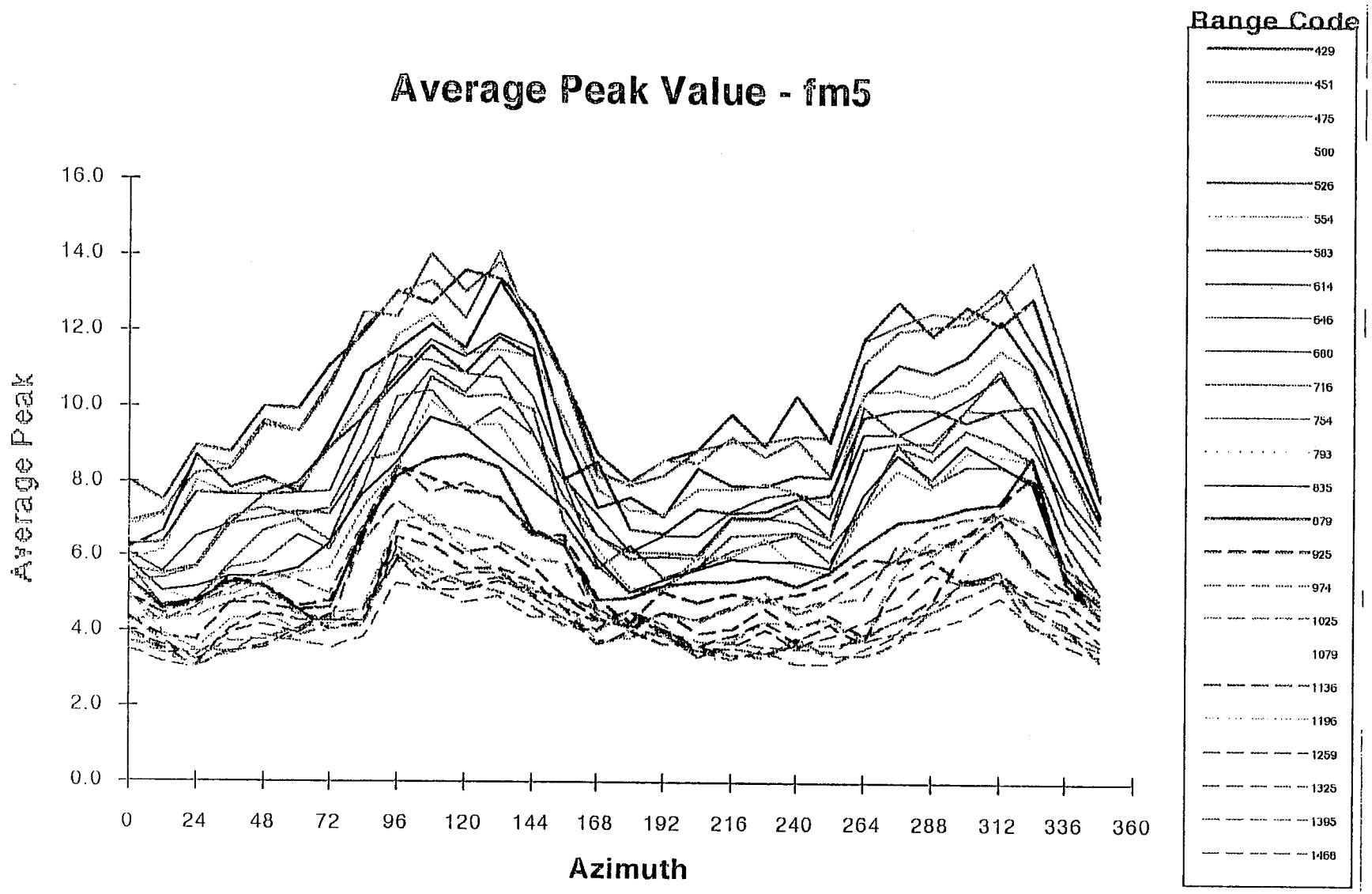
264
276
288


Average Peak Value - fm5
Average Peak
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14.0
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10.0
8.0
6.0
4.0
2.0
0.0
0
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72
96
120
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216
240
264
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312
336
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Azimuth
Range Code
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475
500
526
554
583
614
646
680
716
754
793
835
879
925
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1196
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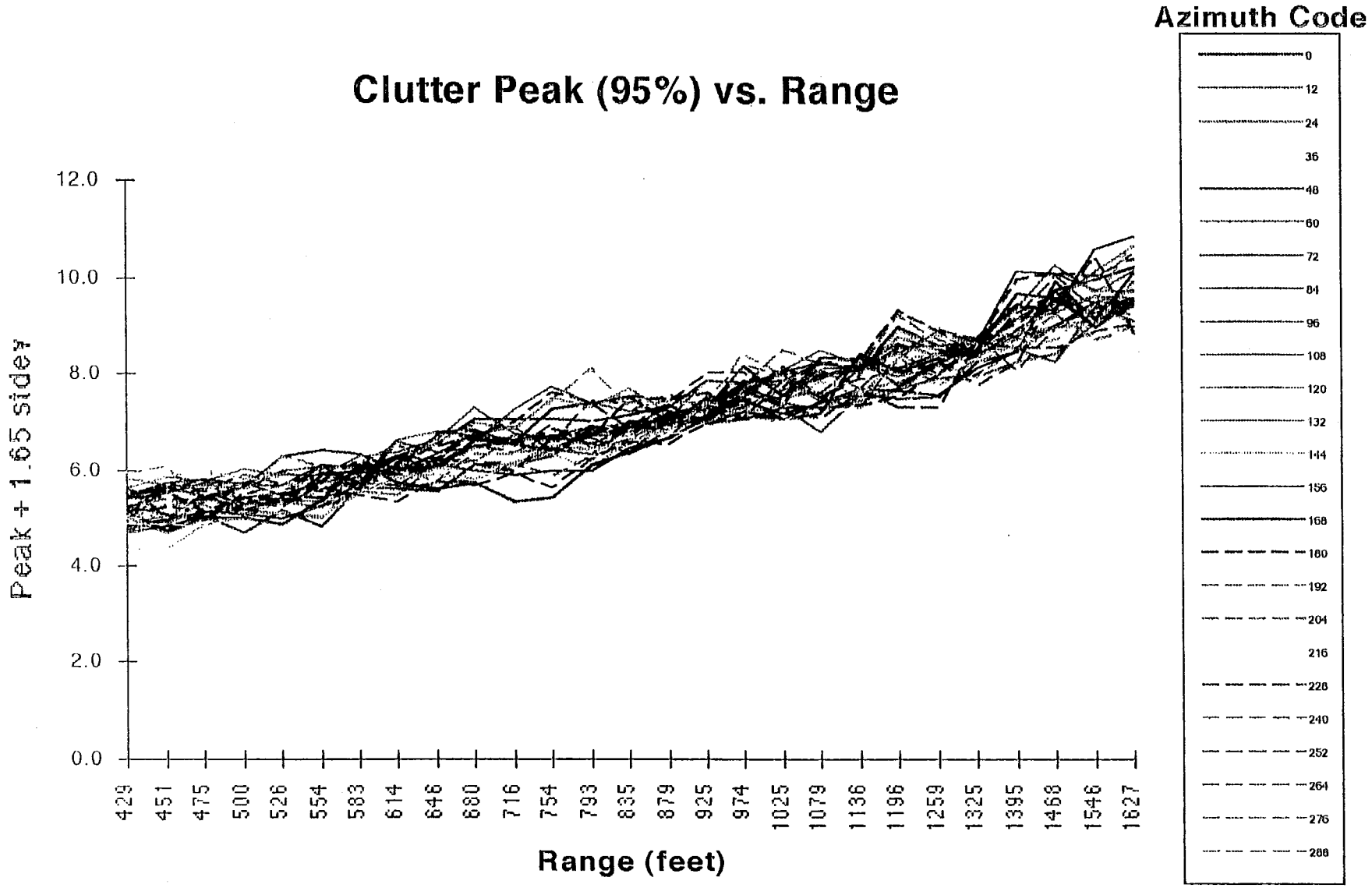
1325
1395
1466

Figure 3-3


Clutter Peak (95%) vs. Range
Peak + 1.65 sider
12.0
10.0
8.0
6.0
4.0
2.0
0.0
429
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475
500
526
554
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614
646
680
716
754
793
835
879
925
974
1025
1079
1136
1196
1259
1325
1395
1468
1546
1627
Range (feet)
Azimuth Code
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Figure 3-4

Once the correlation values have been characterized as a function of viewing aspect and range, it is useful to characterize the clutter (noise) to evaluate whether sufficient margin exists for successful thresholding. Captive carry images were used in which the targets had been electronically erased to yield images representative of clutter that could be expected. Figures 3-4 shows a plot of the maximum clutter peaks vs. range for the full set of TOPS filters.

Figure 3-5 - Tower Test Video Image

Figure 3-6 - Preprocessed Image of Figure 3-5

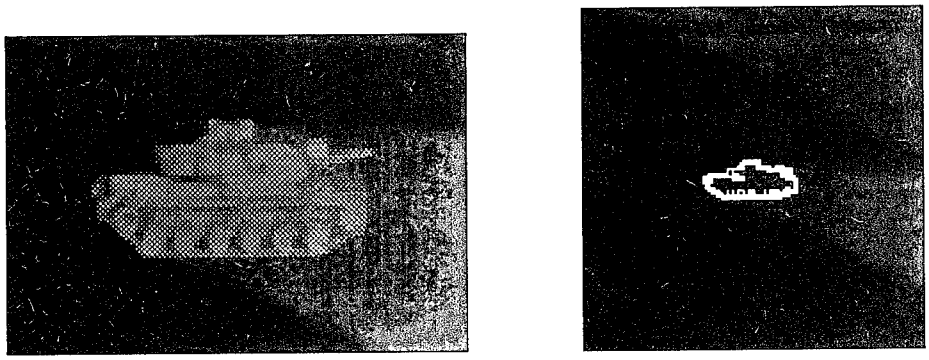


Figure 3-7 -(A) Reference Image close to Figure 3-5 (in terms of distortion);
(B) Preprocessed Reference Image close to Figure 3-6

Filtering Limitations

One of the chief limitations to the system's overall performance was the difference in lighting between the turntable data collection and the real world scenes. In the turntable data collection, the tank was tilted (representing different elevation angles to the sensor) toward the sky. The sun and bright sky therefore illuminated the inside of the treads so that no shadows were present in the interior of the tank (see Figure 3-7 A). In the real world images, dark shadows were almost always present since the tank was always sitting on the ground with a considerably different orientation relative to the sun angle. The resulting binarized images for the two situations differed in that in the real world images the top of the tread was the most significant edge extracted, while in the reference images that particular edge rarely (if ever) showed up (see Figure 3-5 and 3-6). The strongest edge that showed up in the reference images was always the border of the tank, due to the significant differences from the black background (see Figure 3-7 B).

Another related shortcoming in the differences between reference and real-world imagery was due to obscuration of the bottom of the treads in the real world. Even relatively short grass altered the outer border of the tank (as already mentioned, one of the strongest edges in the reference imagery) since it obscured the bottom edge of the treads (see Figure 3-6).

In short, pattern matching can only occur if the patterns can be matched. Considering these limitations the TOPS filters performed exceptionally well in detecting targets at ranges of up to 6500'. The signal to clutter performance of the filters was typically near 3 dB which was more

compared to a pre-defined threshold to establish the probability of the existence of a target at that location.

The second algorithm is referred to as the convolution algorithm and was used exclusively in the TOPS testing. It involves the use of a rounded 7x7 convolution kernel. The convolution kernel is weighted with values that are positive and negative with an approximately zero mean. The convolution kernel slides over the correlation response and multiplies its weight by the correlation plane value and sums all the elements in the kernel. This becomes the value of the convolution response being created on the fly. At the end of the scan the convolution operation has created a new image which is characterized by the elimination of most large areas of constant illumination and many effects of random salt-and-pepper noise. This leaves a response that is searched for local maxima to indicate the location of potential peaks. The raw correlation plane is also searched for local maxima to provide a second location for valid correlation peaks. The coincidence of the two locations has been demonstrated to be a very good estimation of a valid peak.

The postprocessing operators are implemented in a single custom printed circuit card using field programmable logic arrays and high speed convolver circuitry. The custom hardware to implement this algorithm is designed by Martin Marietta to use Harris Digital Signal Processing chips and Xilinx Logic Cell Arrays so it can be configured to perform many functions using many different parameters and kernel values. When the card initializes, the Xilinx chips load themselves with the configuration/algorithm selected by moveable jumpers on the board from an EEPROM. The postprocessor fully supports the processing of the SPOTR camera output at rates in excess of 800Hz for both algorithms. The output of the postprocessor is the input image and filter identification numbers, the x and y locations of up to 10 targets in the input, and a measure of confidence for each target detection. More targets can be identified in any give scene with a corresponding penalty in maintaining the an 800 Hz throughput rate. Additional information on the postprocessor is included in Section 5.0.

5.0 System for Passive Optical Target Recognition (SPOTR)

The deliverable pattern recognition hardware for the TOPS program is called the System for Passive Optical Target Recognition (SPOTR). The SPOTR was designed to satisfy various derived performance and physical requirements. The performance requirements were developed based on the FOG-M missile dynamics and a useful target detection for a gunner. The physical requirements envelope both survival and operational conditions associated with the UH-1 helicopter. The physical size and weight goals were defined to support the remotely piloted vehicle proposed by Eglin AFB for their OSCAR correlator flight testing. Table 5.0-1 illustrates some of the as-built specifications for the SPOTR.

Table 5.0-1. SPOTR As-Built Specifications.

SPACE BANDWIDTH PRODUCT	128 X 128
CORRELATION FRAME RATE	> 800 FPS
PEAK POWER AVERAGE POWER	< 126 WATTS < 76 WATTS
VOLUME	< 1 CUBIC FOOT

WEIGHT	< 43 POUNDS
VIBRATION (OPERATIONAL)	UH-1 + 6dB
THERMAL (OPERATIONAL)	48 - 108° F
SLM FRAME RATE	> 2000 Frames/Sec
SLM PIXEL PITCH	30 μm
SLM ARRAY CONTRAST	20:1
SLM OPTICAL EFFICIENCY (0-ORDER DIFFRACTION EFF. x PHASE MODULATION EFF.)	7%

The SPOTR optical subsystem and electrical subsystem are integrated together using five blind mate connections to minimize cable lengths and processor footprint. The connectors are aligned with guide pins and requires a modest amount of mating force. The interface is solidified with a number of fasteners. The illumination source for the SPOTR is a 690nm laser diode which has been packaged to support the required beam parameters which are driven by the 128x128 ferroelectric liquid crystal (FLC) spatial light modulator (SLM) technology developed by Boulder Nonlinear Systems and the output 128x128 high speed camera developed by DALSA. We have selected an open air discrete component packaging approach for the SPOTR. This approach allows for the adjustments necessary to maintain a diffraction-limited optical system when accounting for the tolerances of off-the-shelf components while maintaining the ruggedness to operate under the UH-1 environment. In addition, this architecture allows for multiple diagnostic port holes into the system for system fabrication and troubleshooting. The electrical subsystem includes the remaining configuration items which is accomplished with 10 printed circuit cards and the embedded CPU controller. The SPOTR is powered by standard 110 VAC or by 28 volt dc via a power inverter with all necessary regulation and filtering contained within the processor. The electrical subsystem is controlled by a set of executive control software and various device drivers which have been designed to operate based on a hardware interrupt handling basis. The software has been designed and demonstrated to operate at the maximum throughput supported by the hardware configuration items.

5.1 Electrical Subsystem

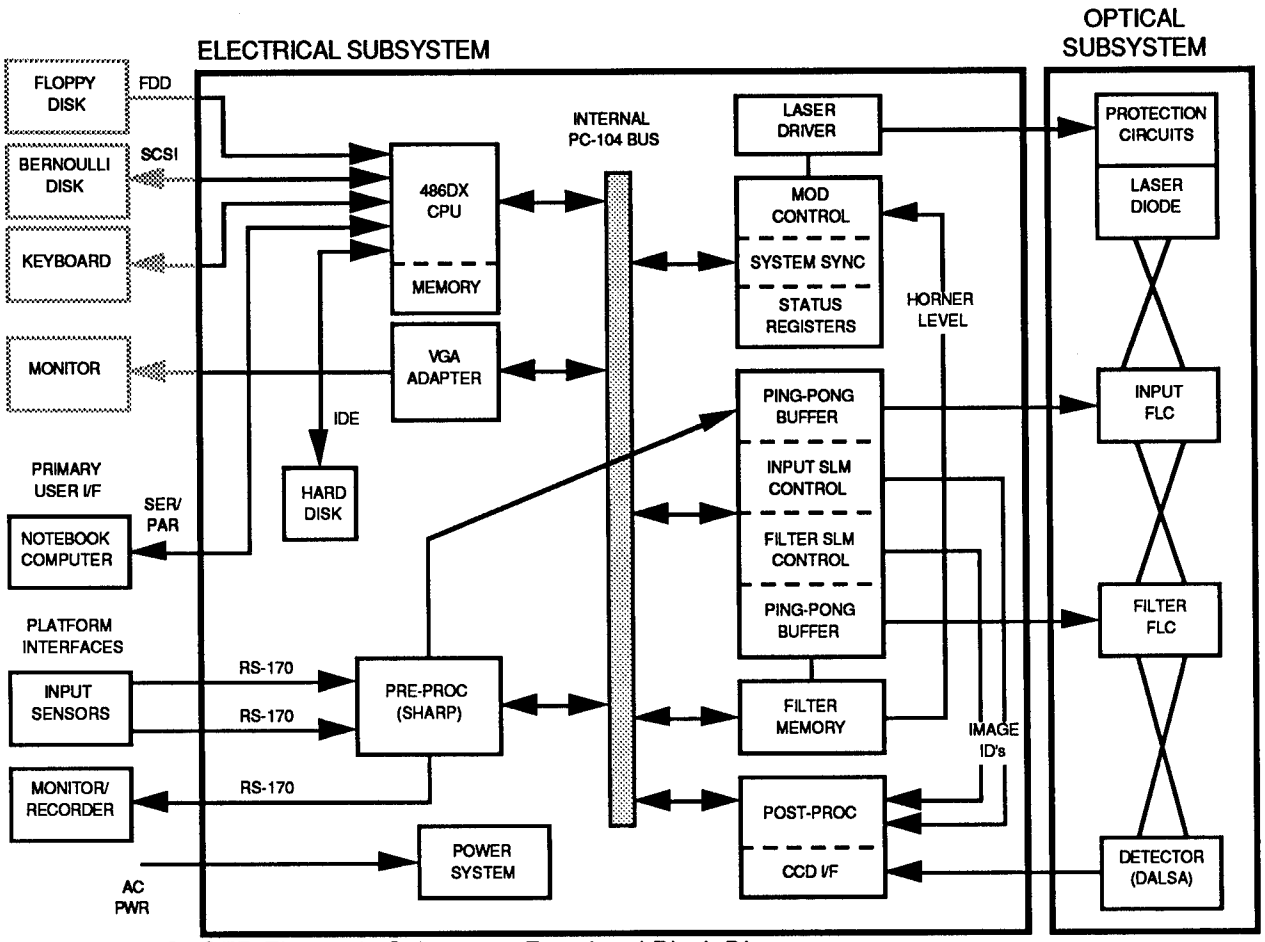


Figure 5.1-1 SPOTR Electronic Subsystem Functional Block Diagram.

The electrical subsystem illustrated in Figure 5.1-1 houses the embedded controller (CPU), preprocessing and postprocessing functions, all the drive circuitry for the laser diode, SLM and detector, and the power system which provides a regulated power source for the system.

The overall electrical control subsystem design philosophy was one of maximizing circuit density and minimizing power consumption while making use of commercial off-the-shelf (COTS) components. However the use of more reliable components and packaging techniques was required to ensure flight worthiness. Finally, within the constraints just stated, it was also desirable that as much operational programmability and flexibility be provided as possible to support on going system development, algorithm modifications, and demonstration activities.

CPU

As an embedded controller, a COTS processor board was chosen from Ampro. The product is based on the PC-104 standard, which is essentially a miniature version of the common ISA personal computer standard and offers a great deal of flexibility through the availability of numerous "stack up modules" by several vendors. The basic CPU is an Intel 486DX-33MHz processor. All typical PC interfaces including IDE disk drive, floppy disk, and serial/parallel ports are provided on the single 5.75" x 8.0" circuit card. Other features include a SCSI interface and up to 16 Mbytes of on board RAM, although this system used only 4 Mbytes of RAM so as not to

conflict with the filter memory discussed later. A display interface is provided by a SVGA adapter (3.6" x 3.8") "mini module" which stacks on top of the CPU card nestled between the memory modules and the interface connectors. Although the system has ROM sockets capable of eventually providing ROM based operating system and executable code, it is currently running as a conventional PC using DOS 6.2 as an operating system.

Non-volatile data storage and "boot disk" is provided by a Ministore 85 Mbyte hard disk. The disk is a miniature 1.8" format and is ruggedized to withstand 200g shock levels. This is accomplished through Minstore's use of built-in accelerometer circuitry which temporarily retracts the write heads when environmental shock reaches levels that could damage the media. An added benefit was the units small size (2" x 3" x 0.5") and weight (2.6 oz).

All the CPU interfaces are provided externally to allow for easy use of conventional keyboard, monitor and disk peripherals to support system development and software debug activities. These interfaces are not however required for normal field operation of the system. The primary user interface consists of front panel "start", "stop" and "reset" push buttons and "search" and "track" mode LED indicators. Extended user access to mode controls and output data is provided by a separate laptop computer running Windows based graphical user interface (GUI) software. The link to the laptop machine is provided via the serial port and is required for current software operation to issue basic operating commands and to adjust various operational variables.

Preprocessor

The preprocessor receives live analog video, converts it into digital format and performs subsequent image processing to reduce the original 512 x 480 pixel gray scale imagery to 128 x 128 pixel binary images that are bit interlaced in a format suitable for direct transfer to the input SLM. The steps to accomplish this begin with first discarding every other frame of the interlaced video signal and then performing a pixel averaging to reduce the image to a 128 x 128 size. The image is then binarized and bit interleaved to FLC format. The results of preprocessing algorithm studies have been discussed in Section 2.0 and in previous reports.

The preprocessor is also used as temporary storage of the input imagery, while correlation results are gathered and processed by the rest of the system. When "targets" are identified, the preprocessor can be supplied the correct X/Y coordinates and used to superimpose a "crosshair" or other indicator on the original input scene. The composite output is then provided in NTSC format for display or recording and subsequent evaluations.

All of these functions are performed by a single commercial General Purpose image processing Board (GPB) from Sharp, Inc. The main printed circuit board contains four banks (three color planes each) of high speed VRAM each capable of storing a 512 x 512 pixel image. The memories share an internal high speed 25 MHz data bus. This internal data bus is also used to supply data directly to the correlator input FLC driver circuitry. A smaller "piggyback" board contains custom ASIC circuits which are capable of performing any of over 250 image processing/transfer functions as direct library function calls by the main correlator control software. A second "piggyback" card known as the WARP card provides for lookup table-based pixel manipulations and is instrumental in performing the FLC interleaving step among other things. The main board plus the two piggybacks make up a standard size PC/AT plug-in card assembly. The card has been customized to provide for both input and output of standard NTSC video signals.

The preprocessor is the largest single card in the electronic subsystem and therefore drives the overall length of the electronics package. It is also the largest single power consumer in the system, requiring up to 30 watts for operation. However, in return for this penalty, an extremely flexible and capable module is provided that can provide image preprocessing of many conceivable types of sensor inputs for many different applications.

Postprocessing

The postprocessing function takes care of gathering the raw image data from the detector CCD synchronously to correlator operation at up to 833 Hz. As discussed in Section 4.0, each image gathered is buffered and can be processed by various possible algorithms to identify correlation peaks. The current algorithms include a "shape finder", a custom rounded 7 x 7 convolution and a two pass convolver plus local maximum algorithm. The last approach has yielded the best results to date. Selection between the algorithms is completely under software control.

For each detector image gathered, the selected algorithm is run to identify any correlation peaks. When a peak is detected, its X/Y coordinates within the 128 x 128 image, its "figure of merit" or confidence factor, and the responsible input and filter frame IDs are collected and put into a "results" FIFO buffer. Any number of multiple correlation peaks per frame are reported and recorded as they are detected. When results are present in the results FIFO, an interrupt flag is set for the CPU to gather the data and process as the current mode of correlator operation might dictate. The postprocessor can sustain this processing rate at up 1000 Hz, well in excess of the 833 Hz maximum detector speed which is the bottleneck for the sustainable end to end processing rate. The only system limitation is the response time of the CPU in collecting and acting upon the results data. The postprocessor can easily swamp the CPU with data if results thresholds are set too low. For most images processed the processor can be operated at maximum throughput without risk of overload.

The postprocessor is also capable of grabbing and storing for subsequent display or file creation by the CPU any occasional raw detector output image "snapshot". Since this activity consumes CPU time and bus bandwidth, a maximum rate of approximately 10 Hz is attainable while other correlator system tasks are running. In addition, a noise frame buffer can be loaded with a predetermined image and automatically subtracted from each incoming detector image before it is submitted to the peak detection algorithm. This may be valuable for instances in which a constant source of noise occurs in the optical system which would consistently be interpreted as a target detection. The use of the this function will prohibit the detection of any target in those areas of a frame for which the noise frame has been defined with high values. This noise frame subtraction process is accomplished with no slow down of other postprocessing functions. The noise frame was not used in the TOPS testing.

All of this capability is also implemented on a single 5.75" x 8.0" circuit card using two Xilinx FPGA devices of 5,000 and 8,000 equivalent gates respectively, in conjunction with five separate 3 x 3 convolver ICs from Harris Semiconductor. This approach provides an unequaled level of performance, and the ultimate level of software control and diversity for future enhancements of postprocessing algorithms.

FLC Drivers

Circuitry to control both the input and filter plane FLCs is contained on a single 5.75" x 8.0" card that is designed to stack on top of the Ampro CPU card footprint. The card contains all clock generation circuitry needed to transfer images to the SLMs via dedicated 16-bit wide interfaces. Extensive circuitry is also provided to offer software control of many different modes of operation including frame rates, laser modulation, and system synchronization. Circuit density is maximized using two separate Xilinx Field-Programmable Gate Arrays (FPGA) of 5,000 equivalent gate complexity to implement the design.

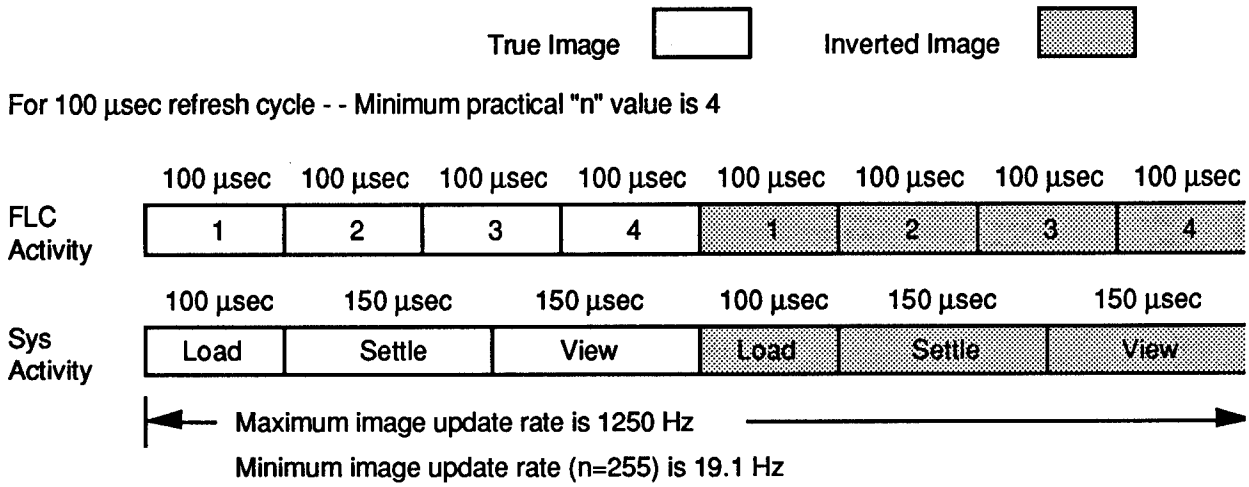


Figure 5.1-2 FLC Timing Diagram.

Since the FLC devices are dynamic in the sense that they require continuous update or refresh of the image on the device as well as periodic image inversions to prevent charge biasing, a 2-port memory approach was used to supply image data to the SLMs. High speed 2-port SRAMs large enough to hold two complete 128 x 128 images are used as data buffers between the SLMs and the rest of the system. The "output" side of the 2-port memory is used to supply data to the SLM at a continuous 100 µsec refresh rate, while the "input" side of the 2-port memory is used to accept the next "new" image to be transferred to the SLM, at whatever data rate it is available. Depending on the selected mode of operation, the 2-port memories are "ping-ponged" synchronously to the frame boundary, as new input images are available. In this context a "frame" is defined as "n" true image refresh cycles followed by "n" inverse image refresh cycles. By varying the value of "n" the frame rate of the FLCs can be software controlled up to 2500 Hz. However, the current system's CCD detector limits system operation to 833 Hz. Figure 5.1-2 illustrates a typical FLC data transfer sequence at 1250 Hz.

The input FLC can be configured to accept data directly from the preprocessor as it becomes available, or from the CPU in the form of "canned" images stored on hard disk. The filter plane FLC can be similarly configured to accept either "canned" imagery under CPU control or images from resident filter image memory described below. Providing images to the SLMs under CPU control is useful for laboratory debug and "demonstration" type modes of operation; whereas, images being provided by the preprocessor and filter memory represent normal "correlator" mode of operation.

Common clock generation circuitry provides control signals for both laser modulation and detector integration that are always synchronous to FLC operation regardless of frame rates and modes of operation. The FLC driver circuitry also provides a 16-bit frame ID word for both the input and filter SLMs. This is subsequently used by the postprocessor for inclusion in the "results" output to

the CPU. This information (i.e.., which input scene and with which filter resulted in a given correlation peak output) can be used to develop and refine filter management software for a wide variety of applications.

Filter Storage

A separate 5.75" x 8.0" card contains sufficient high speed static memory (SRAM) to store 4,000 128 x 128 binary phase-only filters. It is possible to stack multiple memory cards to increase system capacity up to 32,000 filters. The additional memory cards would require some mechanical modification to the existing SPOTR electrical subsystem. This memory array only has to be uploaded once at system power-up or initialization and once loaded is fast enough to provide continuous random access of filters at sustained rates up to 2500 Hz.

Also associated with the filter memory array is a separate Horner Value SRAM that can be used to store a unique 8-bit Horner value for each filter contained in the main filter memory array. The values from this memory, can be used to directly control the modulated laser intensity as each filter is being written to the filter FLC. When a correct range of values are loaded in this SRAM, corresponding to the relative optical efficiencies of the filters being used, the laser intensity can be dynamically varied to partially normalize the intensities of resulting correlation peaks being received by the detector. This lessens the dynamic range required from the detector and somewhat eases the complexity of the postprocessing task.

System functionality is further increased by the addition of a Sequence SRAM and a Sequence FIFO (First In First Out) buffer. These functions physically reside on the FLC driver card but are instrumental in determining the selection and sequence in which filter images are used.

The Sequence SRAM is a 32K x 16-bit look-up table which can be quickly uploaded by the CPU instead of the large array of filter memory itself. The output of the Sequence SRAM is used to determine the physical address of the next filter image instead of simply incrementing locations. It functions therefore as an "indirect address" pointer array that allows all of the filter images stored to be easily accessed in any order and in any repetition sequence desired. Its depth also allows the simultaneous definition of multiple sequences, up to 32K filter images total. In the TOPS testing the complete search, track and reacquire mode strategies were implemented in the firmware/hardware associated with the Sequence SRAM to allow very rapid filter management. The most significant bit of the Sequence SRAM contents is reserved as an End of Sequence (EOS) indication bit. As consecutive locations of the Sequence SRAM are accessed, its contents determine which actual filter is used until a location is encountered where the EOS bit is true. A t that point the address counters controlling access to the Sequence SRAM are reset to a "starting address" value obtained from the Sequence FIFO.

The Sequence FIFO buffer is used to store the starting address of the next filter sequence to be used from the Sequence SRAM. This FIFO is 16 words deep such that up to fifteen consecutive filter sequences can be cued up by the CPU, if known ahead of time, for subsequent automatic processing by the system.. When the Sequence FIFO is empty at system startup, a starting address of "zero" is used. When a single starting address is loaded that address is used until a new value is loaded. When multiple starting addresses are loaded, each one is utilized once until only one remains. This last one is then used repetitively until new starting addresses are downloaded by the CPU.

This memory configuration offers the ultimate flexibility to support future development of sophisticated filter management schemes. All of the memories described above are directly read/write accessible by the CPU for upload and reconfiguration of data. In spite of their high speed and large size, advanced components and MultiChip Module (MCM) packages allow a surprising circuit density. Inherent power strobing features allow the memories to remain in "standby" except when actually being accessed by the system. Thus power consumption is also kept to a minimum.

System Synchronization

A fourth 5.75" x 8.0" circuit card houses several miscellaneous circuit functions needed to complete the electronic control system. These include detector control, laser control, interrupt generation and voltage/temperature monitoring. In the TOPS demonstrations the laser and detector are synchronized with the filter plane SLM such that the laser only illuminate when there is a fully written input and filter plane.

The most significant of these functions is that of CPU interrupt generation. Again to offer the maximum in system flexibility, interrupt generation is implemented in an Event SRAM lookup table. Inputs to the SRAM consist of twelve different "latched" system signals; three front panel switches, two postprocessor results FIFO flags, three FLC timing signals, preprocessor video sync, and three separately programmable hardware timer outputs. Any combination (or combinations) of these twelve input signals can be decoded and returned to the CPU via a dedicated interrupt request line on the ISA bus. Three other output bits of the SRAM are used as separate but simultaneous event decodes that can be used to trigger the three resident hardware timers. Any possible interrupt definition scheme can be determined at system initialization by uploading the contents to the Event SRAM. After initialization, each of the inputs to the Event SRAM can also be dynamically enabled, set or cleared by the CPU. This system allows the ultimate flexibility in interrupt definition and response tailoring.

The system synchronization card also contains programmable controls for laser modulation. On board D/A circuitry and transimpedence amplifier provide a calibrated method of commanding a precise optical output of the systems laser diode. Overall laser system enables are CPU controlled. The On-Off modulation of the laser can also be determined either by direct CPU commands or, as used in the TOPS it can be synchronized to view time control signals received from the FLC drivers to perfectly synchronize the laser with ongoing FLC activity. The "Off" or "DC" level of the laser can be CPU controlled to be any achievable value including zero. This allows the laser diode to always be operated in a coherent mode rather than turning it completely off. Similarly, the "On" or "AC" level of the laser can be CPU controlled to any level, but can also be setup to be determined dynamically using pre-loaded contents from the Horner Value SRAM discussed previously.

Detector synchronization is also provided with a similar degree of programmability. Three modes of operation include free-running at the maximum CCD rate (833 Hz), synchronized to FLC activity, and synchronized to preprocessor video rate. These modes are completely under CPU control while the system sync card provides appropriate pulse shaping and control to always insure proper detector operation. For the TOPS operation the detector has been synchronized to the FLC activity.

Power System

The power system is designed to run off standard 110 VAC input. The 110 VAC is filtered and converted to 150 VDC, which is then distributed to numerous small DC-DC switching converter hybrid circuits that provide the various regulated DC voltages required by system components. Further ripple attenuation filters are provided to insure very noise free power source to sensitive system components such as the FLCs and DALSA detector CCD. The entire system is designed by Martin Marietta using off the shelf hybrids.

The hybrid circuit approach provides a very densely packaged power system capable of delivering up to 200 watts of output with a 76% efficiency. Ripple is maintained at less than 3 mV peak-to-peak. The peak power draw of the processor is 125W. This condition would require 100% usage of the systems capabilities at nearly a 100% duty cycle. It is not obvious that this condition could ever be realized and is currently not possible with the current software package. The average total system power consumption is currently 76 watts when operating the TOPS software at full rate. Minimum power consumption has not been measured.

Control Approach

As seen by the previous hardware descriptions, all image processing and data handling tasks performed electronically, from the video input, through preprocessing, and input FLC control are handled by dedicated high speed hardware. Similarly, the tasks of filter routing to the filter plane FLC, detector output collection, and correlation peak postprocessing are also accomplished by dedicated high speed circuitry. All critical system synchronization and timing is achieved by dedicated hardware interfaces, although most aspects of system operation are completely software programmable if functional flexibility is of higher priority than throughput.

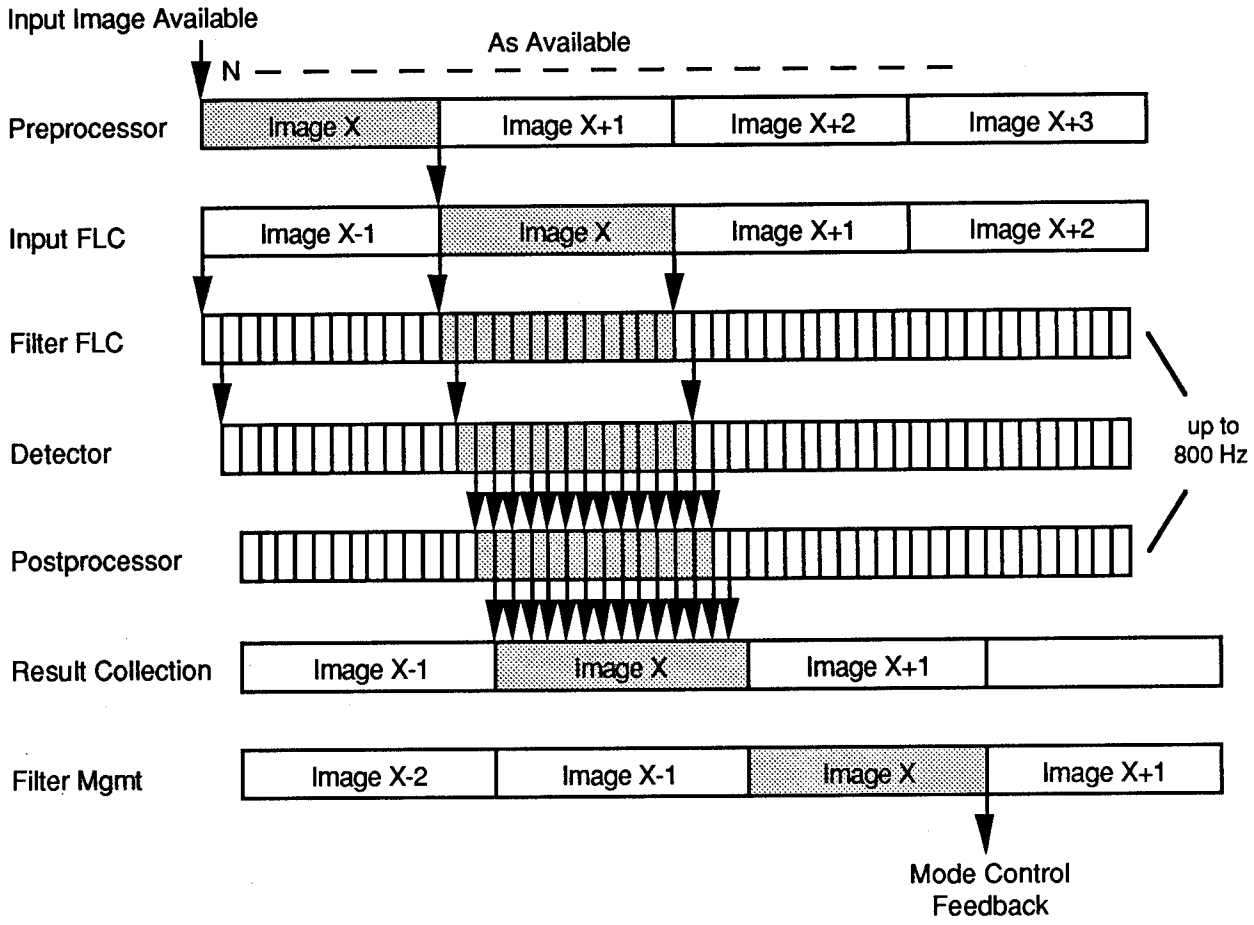


Figure 5.1-3 System Operation Timing Diagram Example.

The inboard 486 CPU is used solely as a housekeeping processor and communicates with all of the other dedicated electronic components via the ISA standard computer bus. System initialization and mode control is accomplished as needed by the CPU sending a few words of control data to each component or transferring data files from the internal hard disk to resident memories. After this initial setup is accomplished, with the exception of the preprocessor, no further action is needed from the CPU until mission environments dynamically require different filters or modes of operation from the system. When this becomes the case, normally only a few words of control data need to be updated by the CPU. This update is often accomplished with a few key strokes on the laptop controller communicated over the serial port interface. This overall control approach allows very fast overall system operation in obtaining correlation "results" and frees up the maximum amount of CPU time for use in filter management and mission management tasks. A timing diagram of only one possible scheme for overall system operation is shown in Figure 5.1-3.

There is a great deal of parallel processing that is achieved by the system due to the fact that each of the major processing components are performing their respective tasks simultaneously in a waterfall manner. The shaded area of Figure 5.1-3 represents one complete correlation process. However, this process is overlapped by both the last pieces of the previous process and the first pieces of the subsequent correlation sequence.

Incoming images on the NTSC input(s) are first digitized and captured by the preprocessor. When a complete gray scale image is available, the preprocessor then completes its algorithm at up to a 15 Hz rate. At that point another input image can be accepted. Once the preprocessed image is available, it is transferred to the input FLC synchronously to ongoing FLC frame boundaries and the currently selected filter sequence is ran at up to 800 Hz frame rates. For each filter in the sequence, the laser is modulated, the detector CCD exposed, and the detector's output image is collected by the postprocessor. The postprocessor, while the next filter is being written to the filter FLC, is analyzing the detector output for peaks and storing any results data into a buffer which is then collected by the CPU and evaluated in support of making filter management decisions in selecting subsequent filter sequences or possibly changing the optical processor's overall mode of operation.

Any CPU directed changes to filter sequences or modes of operation are always delayed to occur synchronously to FLC frame boundaries or filter sequence boundaries. This is done to insure that all correlation results are always reported with accurate information with respect to which input imagery and which particular filters were responsible for their generation.

Physical Configuration

The physical layout of the electrical subsystem is shown in Figure 5.1-4. All of the custom designed circuit cards described previously stack on top of the CPU to form a "stack" which is 5.75" x 8.0" x 3.75", including its mounting frame. The subsystem occupies 864 cubic inches and weighs 23 lbs. First, against the optical subsystem mounting plate is the CPU with its SVGA adapter module sandwiched on top. Next in the stack is the postprocessor card. This is followed by the FLC driver card and the filter memory cards. On top of the stack is the system synchronization card. All card to card electrical interfaces are achieved through "stack" headers like the one visible along the top edge of the card stack. This approach minimizes the use of discrete cabling and improves the overall interconnect reliability of the system. This card stack, with its integral card frame and rear panel, provides all external interface connections to the CPU as well. Situated underneath the cabling to the rear panel is the miniature hard disk. Thus the card stack assembly provides all system electronic functions except for preprocessing and laser current regulation.

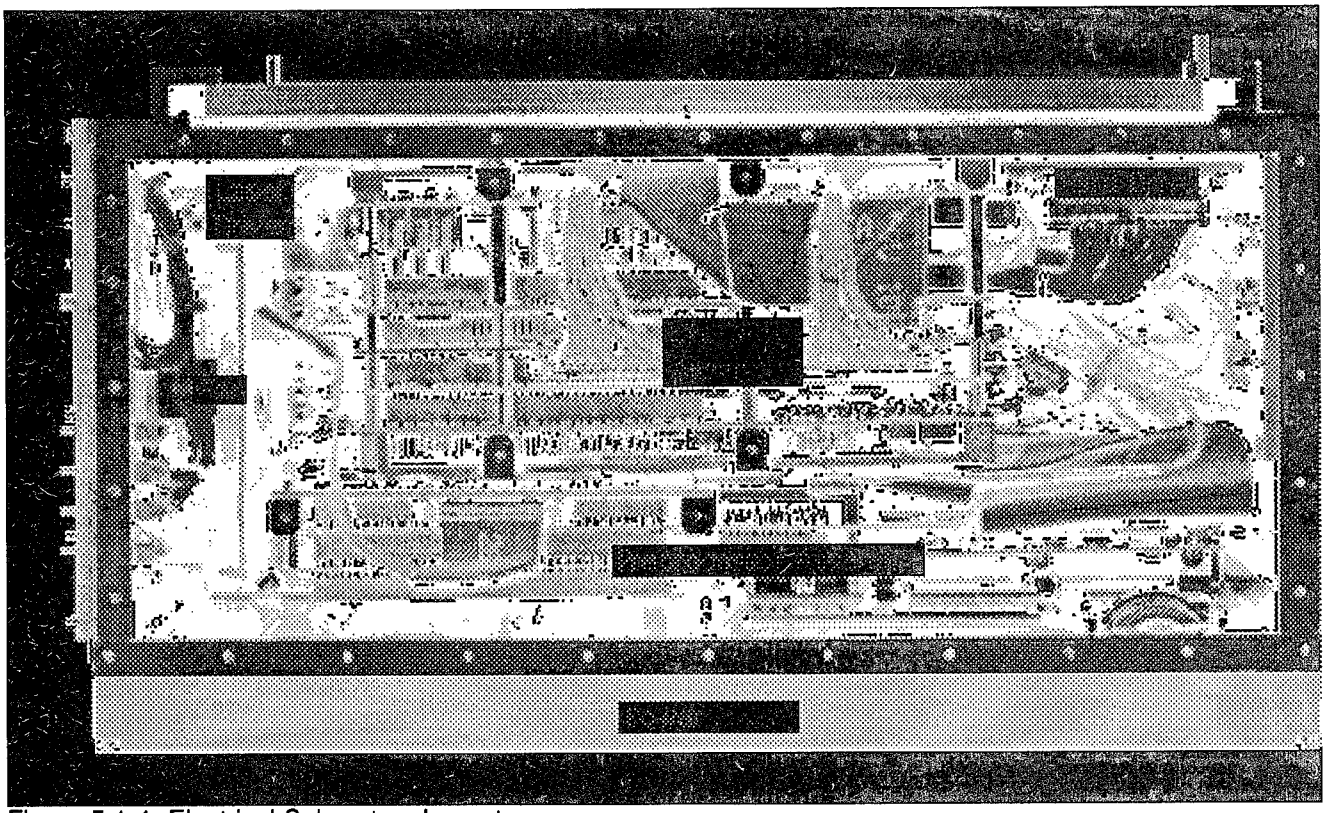


Figure 5.1-4 Electrical Subsystem Layout.

The Sharp preprocessor card is located in front of the stack. CPU bus connections to it are provided via folded, shielded ribbon cables from the front of the card stack. Its data interface to the FLC driver is also achieved through ribbon cable connection, as can be seen at the left end of the card stack in Figure 5.1-4.

The power system is 1.5" thick and forms the front wall of the electrical housing. Its regulated DC power outputs are provided through connections at the bottom of the assembly to a single power distribution card which is mounted in the bottom of the chassis. Thermal dissipation from the power system is accommodated by conduction paths through the front wall assembly down through the bottom edge and directly into the chassis bottom plate. A single fan draws air in the left end of the chassis, forcing it through the circuit cards in the stack and the preprocessor before exiting through the top cover towards the right end.

Enabling Technologies

As mentioned briefly in the previous descriptions, the use of state-of-the-art components and packaging technologies enabled us to achieve this rather impressive electronics packaging density with relatively low risk. The key technologies used were high density surface mount components (SMT), multichip module components (MCM), and the Xilinx Field Programmable Logic Arrays (FPGA).

The use of fine pitch surface mounted components allowed nearly double the circuit density achievable with conventional surface mount components. Fine pitch refers to lead spacing of 20-25 mils as opposed to the standard 50 mil pitch components. "Double Density" parts made by Integrated Device Technologies allowed the incorporation of 16-bit bus oriented buffering and

multiplexing circuitry in the same printed circuit area as required by 8-bit wide functions in standard SMT components. Also the Xilinx FPGA components and some of the memory components were available in "fine pitch" versions.

The filter memory card took advantage of available COTS memory components manufactured by Dense Pac Microsystems, Inc.. The multichip modules offer 1 Mbyte of high speed, low power SRAM in a single low-profile through-hole mounted assembly. A multilayer ceramic substrate is used as a miniature printed circuit assembly, to discrete fine pitch (15 mil) memory ICs are mounted on both sides of the substrate and connections are routed to interface pins at the edge of the substrate.

The Xilinx FPGAs used were as large as 8,000 equivalent gates in a single 208 pin quad flatpak, 20 mil pitch package. This was a very impressive and readily available density at the time of our original design efforts, however even greater complexity devices are available now which go up to 25,0000 equivalent gates of logic in a single device. The Xilinx technology not only allowed us to achieve impressive system density but also, due to its in-circuit reconfigurability, allowed us to iterate our firmware designs several times even after the production of the circuit cards without any impacts to board layouts. This proved to be a great advantage to cost/schedule performance.

Future Improvements

In light of the technologies used, several steps can, and should, be taken to further improve both the performance and size/weight/power characteristics of the next generation of correlator controller design.

The first and most significant improvement could be achieved through a redesign of the preprocessor card. Although the Sharp GPB card is a very capable and flexible component, it is actually overkill for the system as it is currently used. As a preprocessor, only 50% of its capabilities are being utilized and a significant size and power penalty are being paid for that unused capacity. A custom designed preprocessor card that is PC-104 compatible and would fit directly on our already existing card stack would be readily possible using the same technology as used in our other card designs. By simplifying the design to provide only the capabilities needed for the correlator preprocessing function, approximately 3 inches of overall length of the electrical subsystem could be disposed of and 20 watts of power dissipation saved.

In conjunction with this, the system synchronization card could be redesigned to use Xilinx FPGA technology as well. Originally discrete logic components were used due to resource and schedule limitations. With a redesign, the laser current source, currently a separate module, could easily be incorporated onto the system synchronization card and its overall "parts count" complexity reduced significantly along with some savings in power dissipation. The deletion of the separate module for laser drive circuitry would also aid in the overall chassis size reduction.

A third improvement would be the redesign of the detector CCD package. The current use of DALSA commercial packaging drives the overall size of the optical subsystem significantly. The specified requirement for "very clean", regulated power could also be disposed of with improved A/D circuitry and self contained power regulation at the CCD itself. This in turn would allow a very significant reduction in our overall power system complexity. Since most of the electronics, other than the CCD, are relatively noise tolerant, several hybrid circuits currently used for ripple

attenuation and filtering could be omitted. An overall reduction in system power dissipation would also allow the use of smaller DC-DC converter hybrids in some instances. A power system redesign could easily be achieved which would be in keeping with the overall chassis size reduction allowed by the other redesign efforts as well as power dissipation reductions.

If all of the above improvements and redesigns were implemented, an overall reduction in the electrical subsystem size, weight and volume of 25% to 35% should be readily attainable. A similar reduction in system power consumption could be expected to approach 40%. An added benefit to this power reduction, would be that forced air cooling of the system would likely no longer be necessary. Packaging steps could be taken that would allow space applications of the correlator to be a reality.

5.2 Optical Subsystem

The optical subsystem is a highly parallel, high speed co-processor in the SPOTR. It is tasked by the electrical subsystem with performing the correlation function as part of the target recognition algorithm. In doing so it performs two 128x128 fast Fourier transforms, complex multiplication of two 128x128 arrays of data, and performs a modulus squared operation on a 128x128 complex correlation plane at the speed of light. It must accept binary images from the input FLC driver at a rate of at least 30 Hz and filters from the filter FLC driver at a rate of at least 800 Hz. When the SLMs are written the laser diode is illuminate which implements the correlation function with the given input image and filter at the speed of light. For the TOPS program, the SPOTR optical subsystem was required to be packaged such that integrity of the processor and the correlation function was maintained under environments induced by a UH-1 helicopter platform and while weighing less than 15 pounds and occupying a volume of less than 1 cubic foot.

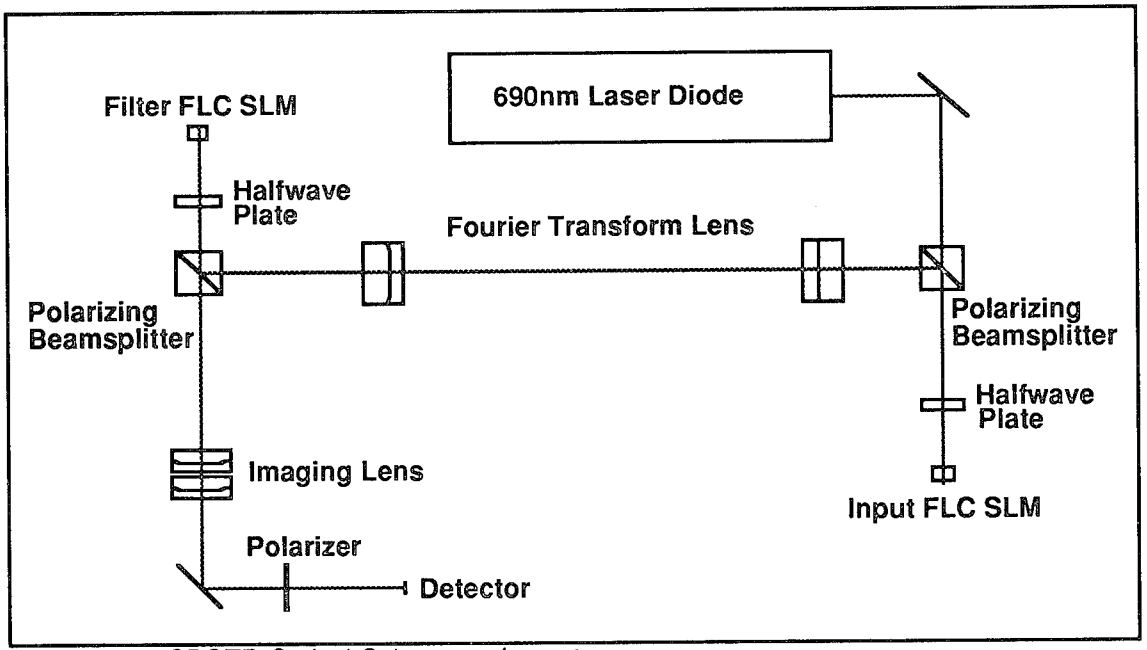


Figure 5.2-1 SPOTR Optical Subsystem Layout.

Table 5.2-1 - SPOTR Optical Subsystem Components.

Component	Manufacturer	Part Number	Quantity
Laser	MicroLaser	SK8975100100-009	2 (1 backup)

Detector	DALSA	CA-D1-0128D	2 (1 backup)
Spatial light modulator	Boulder Nonlinear Systems	128x128	4 (2 backups)
Fold Mirror	CVI Laser Corporation	LDM-690.0-0737-45	2
Polarizing Beam Splitter Cube	Meadowlark Optics	*CTG-BP-0.5-690	2
Half-wave plate	Meadowlark Optics	A50-0.5-690	2
Fourier lens, 250mm FL	Newport Corporation	PAC**SI201314	2
Imaging lens, 175mm FL	Newport Corporation	PAC**SI201354	2

The optical subsystem is based on the principles of a Vander Lugt 4f correlator. The input and filter SLMs are 128x128 FLC devices being operated in the binary phase-only mode. The laser is a 30 mW 690nm diode which has been collimated and expanded to provide a 8 mm diameter beam (FWHM). The detector is a 128x128 CCD capable of 833 Hz sustained throughput. The optics are off-the-shelf except for modifications to the lenses to reduce the diameter from 1.0" to 0.75". The optical layout is shown in Figure 5.2-1. A list of components and there associated model numbers is given in Table 5.2-1 and the prescription is given in Table 5.2-2.

Table 5.2-2 - SPOTR Optical Design Prescription.

SRF	RADIUS	THICKNESS	GLASS	NOTES
1	--	-135.39598	AIR	Laser
2,3	--	30.00000	AIR	mirror
4	--	-44.45000	AIR	
5	--	-12.70000	BK7	PBSC Transmit
6	--	-31.01763	AIR	
7	--	-3.25198	BK7	1/2 waveplate
8	--	-18.06600	AIR	
9	--	-2.00000	BK7	FLC Cover Glass
10	-1.3500E+04	--	REFLECT	#SU 2
11	--	2.00000	BK7	FLC Cover Glass
12	--	18.06600	AIR	
13	--	3.25198	BK7	1/2 waveplate
14	--	31.01763	PAIR	
15	--	6.35000	BK7	PBSC Reflect
16	--	--	REFLECT	
17	--	-6.35000	BK7	
18	--	-21.11914	AIR	
19	-152.73419	-7.53700	BK7	Newport 250mm FL
20	112.99980	-4.02000	SF5	PAC**SI201314
21	338.90546	-106.09370	AIR	S/N 10
22	-339.02730	-4.02000	SF5	Newport 250mm FL
23	-113.03979	-7.53700	BK7	PAC**SI201314
24	152.78910	-49.10656	AIR	S/N 11
25,26	--	-6.35000	BK7	PBSC Reflect
27	--	6.35000	BK7	
28	--	12.54370	AIR	

29	–	3.25000	BK7	1/2 waveplate
30	–	18.06600	AIR	
31	–	2.00000	BK7	FLC Cover Glass
32	1.0000E+04	–	REFLECT	#Orb 13
33	–	-2.00000	BK7	FLC Cover Glass
34	–	-18.06600	AIR	
35	–	-3.25000	BK7	1/2 waveplate
36	–	-12.54370	AIR	
37	–	-12.70000	BK7	PBSC Transmit
38	–	-41.29922	AIR	
39	-106.13552	-3.84500	BK7	S/N 4
40	78.18766	-2.45500	SF5	PAC**SI201354
41	233.27502	-5.34350	AIR	Newport 175mm FL
42	-106.29790	-3.75400	BK7	S/N 5
43	78.31349	-2.54600	SF5	PAC**SI201354
44	233.63191	-24.41247	AIR	Newport 175mm FL
45	–	–	REFLECT	Mirror
46	–	60.98394	AIR	
47	–	0.40000	BK6	DALSA Cover Glass
48	–	2.0979E-07	AIR	DALSA Detector

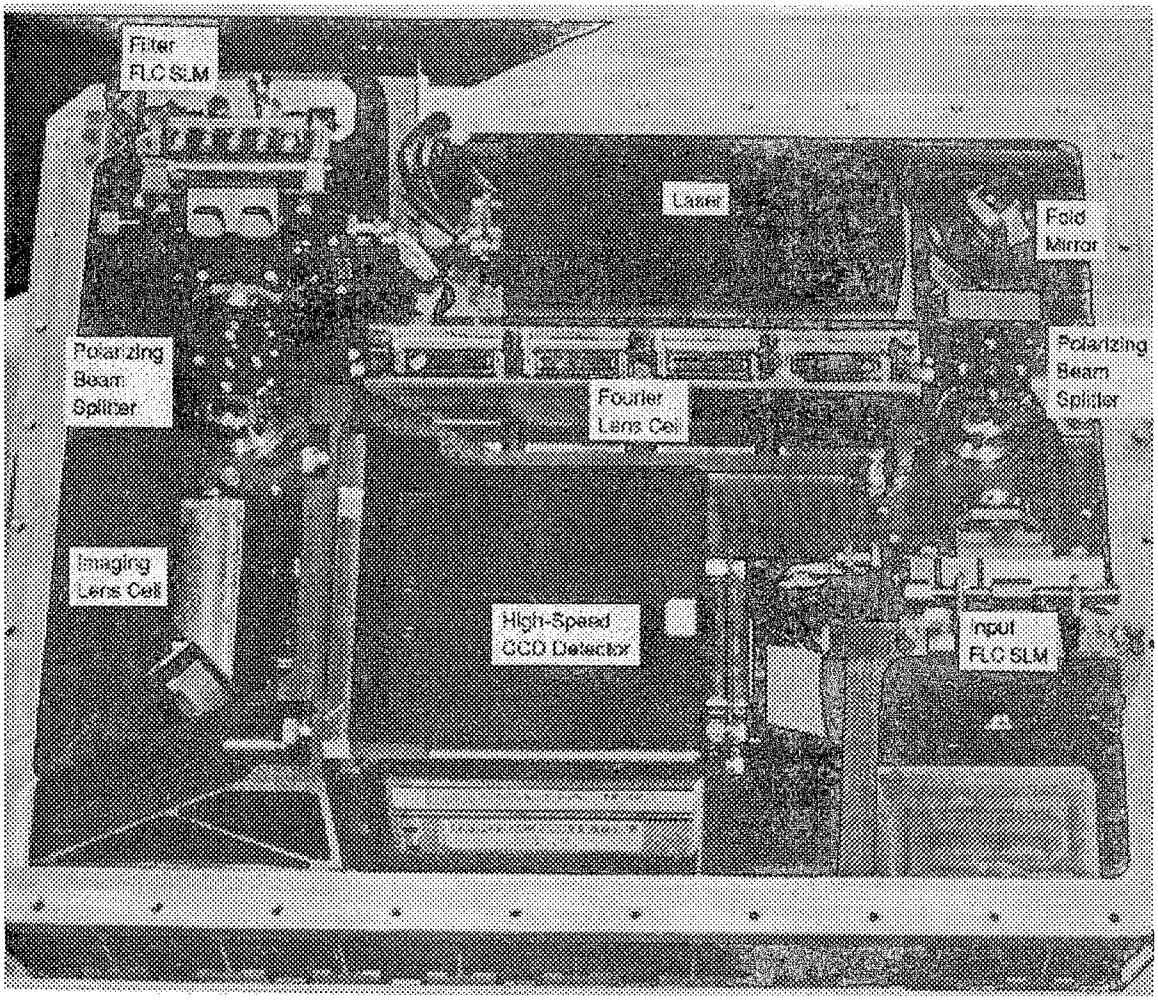


Figure 5.2-2 SPOTR optical subsystem.

The optical path of the SPOTR can be explained in conjunction with Figure 5.2-2. The conditioned laser emission is incident on the fold mirror in the upper right of the figure. The light propagates through the beam splitter and is rotated to align proper polarization onto the input SLM. The SLM is reflective and modulates the light in a binary phase mode (1/2 wave of retardation for one set of pixel settings relative to the other set). The light reflected from the SLM is incident on the beam splitter and is turned 90° to the left through the Fourier lens cell. The second beam splitter turns the light 90° toward the top of the page and incident on the filter SLM. Upon reflection the product of the input transform and binary phase filter modulation is passed through the beam splitter and folded with a mirror through the imaging lens cell and focused onto the DALSA camera.

The optical subsystem mechanical components consist of the optics bed and all mounts associated with placing and holding the optics components. These opto-mechanical components were designed to meet the environments of the UH-1 helicopter platform with a cost-effective approach. The optics subassembly consists of an optical bed with precise mounting points for the individual component mounts. Several individual mounts were used: fold mirror, beam splitter cubes, lens cells, input SLM stage, and filter SLM stage (see Figure 5.2-2). In addition to these mounts the laser and detector were mounted directly to the optics bed. Due to the schedule

constraints of the TOPS program it was necessary to perform concurrent engineering on the optics subassembly. During the design phase the mechanical engineer and the manufacturing engineer worked closely together to ensure that the design could be built in a cost-effective manner. In addition, a vibration analysis was being performed on the optics subassembly to ensure that the SPOTR would function while being subjected to the expected helicopter environments.

The optical design performed as expected. The design was analyzed and demonstrated to be diffraction limited. The correlator performed better than many of the requirements. An example is that the resulting flux budget allows for sustained operating rates of over 800 Hz. The volume of the optical subassembly is approximately half of a cubic foot and the weight of the subassembly came in at slightly over 17 pounds. The correlator performed very well in the Huntsville, AL (mid summer) and UH-1 helicopter environments. The only apparent effect is a change in modulation characteristics of the SLMs due to large temperature changes. These changes were minimized by rotating the half wave plates of the system and adjusting the gain and offset settings of the DALSA camera. If this cannot be corrected during further development of the FLC SLMs then it could be corrected by controlling the temperature of the SLMs.

Several FLC SLMs were obtained and tested. Most of the SLMs that were rejected had either a significant phase curvature (probably a liquid crystal thickness variation) or large regions which were modulating in the opposite state of the programmed modulation. In addition, most of the SLMs have a curvature in the reflective die which causes the SLM to act as a lens. This lens effect is significant enough to cause as much as a centimeter of focus shift in the correlator. Therefore, the curvature of each SLM had to be measured so that the Fourier lens cell could be shifted to correct for the focus shift. These problems appear to be mainly the normal growing pains of any new high technology developmental device. However if a more rigid mechanical architecture, such as solid optics, would have been selected the growing pains would have been much more severe than the few days of engineering time to rework the lens spacers.

5.3 User Interfaces

As illustrated in Table 5.3-1 there are several potential SPOTR interfaces. The laptop computer interface was used to issue system level control signals from the user. The interface was also used for the transmission of new software and data between external development workstations and the SPOTR CPU and peripherals. File transfer between the two computers is accomplished using Laplink, an off-the-shelf commercial product that makes the optical processor's hard disk look like a local disk drive to the user interface. It runs efficiently in the background and works well.

In the field test we used the video input RS-170 interfaces to provide input imagery from the missile seeker to the preprocessor. The video output RS-170 interface was distributed to a video monitor and a tape deck for observing and recording the SPOTR performance. Other interface options include the transfer of digital input imagery and spatial filters via SCSI removable hard disk or floppy disk. These data can be stored on the embedded hard disk or onboard memory.

Table 5.3-1. SPOTR User Interfaces.

		Interface	Comment
Required	486 Notebook Computer	Serial/Parallel	System Operation

	Video Input	(2) RS-170	2 S/W Switchable Video Sources
	Video Output	RS-170	Crosshair Overlay/Correlation Plane Image
	Text File Output	Embedded CPU	x,y, Input & Filter I.D., Figure of Merit
	Hard Disk	Embedded CPU	System Software/Filter Storage
Optional	Removable Hard Disk	SCSI	Large Quantity Data Transfer
	Floppy Disk	Embedded CPU	Data Transfer
	Keyboard	Embedded CPU	Direct Access to Internal CPU
	VGA Monitor	Embedded CPU	Direct Access to Internal CPU

5.4 Software

The SPOTR software is a single-threaded, multi-tasking system. A 32-bit protected mode language compiler was selected (MetaWare High C/C++™) along with supporting extensions to the MS-DOS™ operating system (Phar Lap TNT DOS-Extender™). The source code modularity is based on the natural divisions of functionality necessary to control the hardware within the OPM and perform the captive carry mission. Certain routines are implemented in Intel® 80386 assembly language (Phar Lap 386|ASM™) in order to optimize extremely time critical execution units. The basic set of software requirements are:

1. Fully utilizing the system hardware functionality and capabilities.
2. Real-time, timing deterministic, control of system operation.
3. Dynamic data determined algorithm selection and data manipulation.
4. Capable of supporting multiple operating modes and mission profiles.
5. Interactive user command access.
6. Concurrent and post mission data reduction and analysis.
7. Flexibility to modify mission parameters and to support a variety of missions.
8. Command verification and error detection, analysis, and response.
9. System initialization and termination responsibilities.
10. Disk based parameter input and data archiving.
11. Modular, logical, self-documenting, and re-usable source code.
12. Use of legacy and COTS software whenever feasible.

Device Initialization Module

There are three primary software functional modules. The first is the device initialization module which saves and initializes all hardware and program modules. The device initialization functions are a set of functions that are explicitly placed upon the execution queue in order to setup the hardware configuration so as to satisfy the mission starting conditions. Generally these functions are loaded upon startup and are configured using a parameter file resident on the system disk. All system memories are generally loaded and verified by these routines. Device initialization functions are considered operational level routines and are written in C/C++. Control then passes to the second module, the executive controller "exec".

Exec Controller Module

The exec controller software module is a task scheduler. It examines the task queue for tasks that need doing, and calls a subroutine for each in turn. Designated hardware interrupts cause control to pass to the third software module, the interrupt handler.

Interrupt Handler Module

The OPM system execution timing is based upon hardware determined "events" which provide key sequencing information to the exec software. The Interrupt handler function is the mechanism by which exec software captures these hardware events and modifies the system operation accordingly. Certain predetermined actions, such as the receipt of an input video frame, trigger the system sync card to generate a physical interrupt signal to be generated which is then intercepted by the system CPU. The CPU then immediately suspends its current operations and "jumps" to a special software routine that performs the processing necessary to service the interrupt. In the exec this interrupt service routine does the following:

1. Disables the receipt of all interrupts.
2. Reads the system Sync card event register in order to determine what hardware event caused the interrupt.
3. Places the appropriate processing function at the tail of the function queue.
4. Resets the system Sync card circuitry to receive the next hardware event.
5. Reset the CPU interrupt circuitry.
6. Re-enables the receipt of interrupts.

This method of placing the event processing functions upon an execution queue allows the system to accept asynchronous interrupts very rapidly actually servicing the events in an ordered, sequential fashion. The hardware interrupt handler routine is written in assembly language and is considered to be a system level routine.

This system provides good response speed for attending to hardware interrupts, while minimizing the common problem of having a large untidy stack full of untended interrupts pending. The system is efficient and provides enormous resources for troubleshooting, data recording, and mission adaptation since the exec can modify the task list according to the situation. Each interrupt can be logged when it arrives and again when it is serviced.

Software Functions

The function execution queue is a program structure that receives all of the execution addresses and parameters for all of the OPM operation functions or routines. The exec software continuously examines the execution queue for any pending function. If one is found the function is processed to completion where the execution queue is once again examined. If there are no entries upon the execution queue the system is essentially quiescent. Any executing function may place another function (including itself) upon the execution queue. The execution queue structure is written in C and is a system level routine.

The system operation is determined by the device management functions. These routines are the set of functions that are placed on the execution queue in response to a hardware event or by another function. These routines encompass the management of the hardware during system operation, provide the implementation of the image manipulation and filter management

algorithms, and provide for the processing of user commands. These functions execute during the operational portion of the given mission. These functions are implemented in C and C++ and are operational level routines. These management functions include control of preprocessor, postprocessor, filters, FLCs, synchronization, file I/O and DOS access, front panel functions, and Command Response/Mission management.

Preprocessor management consists of operating the Sharp GPB-1 by calling library routines in the proper sequence. The source for these library routines is maintained by the Sharp Corporation. They have been very cooperative with us, allowing us to recompile their source on our protected-mode compiler.

Postprocessor management is pretty simple once the necessary setup is done, since our custom postprocessor is synchronized based on the DALSA camera timing signals. Results must be read out of the postprocessor results buffer and passed to onboard RAM and to the preprocessor to support the crosshair overlay on the input image. The data collected during a mission is stored as a structure in system memory until the end of mission. In response to a user command and/or at the time of program termination the data archiving function is invoked. The data archiving function takes the memory resident data and transfers it to the system hard disk or other non-volatile storage. Data formatting and engineering unit translation is accomplished within these routines also. These routines are implemented in C/C++ and are operational level. Filter identification is also available to the filter manager to support the sequencing of filters in track and reacquire modes. (This provides insight to target's identity, orientation, scale, etc.)

Filter management consists of tracking a target and computing new filters to try as range and orientation changes. The filters are loaded in memory at initialization but are engaged by writing to sequence SRAM or sequence FIFO. Multiple target hypotheses were processed during the TOPS testing with additional capability available when the application demands it.

Most of the FLC management is performed at system boot-up and initialization. The FLC drivers operate as stand alone modules during a defined operational configuration.

Synchronization management includes such things as determining priorities for interrupts, setting up filter insertion rates, and monitoring health functions i.e. temperatures and power supply voltages.

File I/O and DOS access is generally done off-line (i.e. when the correlator has been commanded to suspend correlations). Results in RAM from the postprocessor and event logs are transferred to files on the hard disk. Note that results are appended to the same control file that was read at startup time. This file can be the basis of remote control for the correlator, as another computer writes this file containing instructions, then reads it back to get the results. It is valuable to have the results prefixed with the setup that produced them for post-test analysis.

Front panel functions include operation under control of Start and Stop pushbuttons on the front of the Optical Processor, and updating of the Status indicator LEDs.

Command Response/Mission management provides a more robust control functionality than the front panel pushbuttons. The command response interface is a special case interrupt service routine (ISR) attached to the serial communications port. Upon receipt of an inbound command character the ISR verifies the command character is valid and then loads the command

processing function upon the execution queue. The received command character is passed to the command processing function for evaluation. The serial command ISR is a system level routine written in assembly language and the command processing function is implemented in C/C++ at the operational level. A serial port is used for functional control of the Optical Processor. One-character commands to stop, start, suspend, change algorithms, etc., are supported. The program termination routines are invoked at the end of a mission scenario, by a user command input, or by a fatal system operation error. The termination routines provide for an orderly shutdown of the OPM so that the system is terminated in a known state, to preclude the loss of collected results data, and to minimize potential damage to hardware. In the event of a fatal exec operating error the termination routine will notify the user of a possible explanation of the error by outputting to the console an error message. These routines are implemented in C/C++ and are system level routines.

Graphic User interface (GUI)

The graphic user interface (GUI) operates on a separate laptop terminal and serves as the main operational interface with connections to the OPM via the RS232 serial and LPT1 parallel interface ports. This implementation allows the exec software to be tightly coupled with the OPM hardware functionality without incurring the unnecessary burden of maintaining the graphical environment and command verification duties that are handled by the GUI. The GUI software is designed to a) compile control files for the Optical Processor software, b) generate serial commands and verify acknowledgment, and c) display results. This auxiliary computer is connected to the Optical Processor by two cables: a null modem between their serial ports, and a parallel link between their printer ports. This design also allows for natural divisions between the human command generation and data reduction interfaces and processors low-level command set and binary data structures. In addition, the GUI host may be physically separate from the OPM or may be supplanted entirely by another interface that adheres to the OPM/ EXEC command and data interface specification. The GUI software was developed using Microsoft's Professional Visual Basic running on Microsoft Windows. This allowed quick and flexible construction of the control panel's appearance and saved huge amounts of coding time, since the language provides a development environment that is itself a graphical user interface, allowing the developer to draw the panels directly and automatically generating much of the coding and interrelationships between various modules. It is planned to overcome some of the drawbacks of the BASIC language by converting this code to C later.

The GUI software is implemented as a single module with five principal user interface screens:

1. Main selection screen.
2. Search mode setup screen.
3. Search mode profile screen.
4. Lab mode config screen.
5. Lab mode inspect screen.

The main selection screen is the principal selection screen presented to the user upon program initialization. The user selects the various menu buttons for OPM setup, operation, and results information. The screen presents the user with an intuitive graphics display of a control panel, allowing the user to "press" various buttons on the panel (by pointing and clicking with a mouse or other pointing device, or by typing "hot keys" on a keyboard.) This control panel is divided into three sections. The upper section was developed to provide mission-specific functions for the

TOPS program. The center section has similar but more general functions for laboratory use. The third section contains controls for selecting algorithms, shutting down the correlator software, and similar items.

Whether operating via the upper or center sections, there are three buttons to press. The one on the left opens a Setup window that lets the user choose elements of the mission setup, save and retrieve the setup, and custom tailor it to a particular situation.

The middle button sends the setup as a file to the Optical Processor, then sends a serial link command for the Optical Processor software to read it and start operations. Pressing this button again sends a serial command to suspend operations and append the results to the setup file. The right-hand button causes the user interface to read the generated setup/results file, open a results display window, and graph the results. In the TOPS operation, knowledge of the filter set allows the graphing of seeker position with respect to target orientation.

The search setup screen allows the user to input the initial mission parameters which then creates the mission initialization file for the exec software. Various setup files can be stored to disk for future use.

The search profile screen allows the user to graphically view the results data from a stored mission data file.

The Lab config screen allows the user to setup the OPM hardware in a manner conductive to laboratory investigations. Similar to the search setup screen, the lab config screen creates an initialization file to be read by the exec software.

The laboratory mode inspect mode graphically displays results collected in laboratory experiments.

Software Performance Summary

The software performed as designed. The throughput latency of the interrupt service routines was excellent and the overall system software performance met the captive carry mission needs. The GUI software was not mature enough to support the captive carry mission. Adequate user interface support was achieved through the use of COTS terminal emulation software and commands used from key strokes on the laptop terminal during flight.

Recommended Areas of Continued Software Development:

Evolution of the exec and GUI software is necessary to support further applications of the SPOTR either in additional field testing or in the laboratory. Some suggested areas of improvement are:

1. Exec code port to Microsoft Visual C++™. This language product supports superior development environments and allows for inline assembly routines thus eliminating the need for a separate assembly language product. Superior debugging tools are also supported.
2. Redesign the software model to adhere to object oriented design and coding standards. Emphasize code reusability.

3. Optimize the preprocessor function library to provide more consistent input image timing and reliability.
4. Enhance and expand the internal error detection and reporting software.
5. Enhance and expand the laboratory mode flexibility and capabilities.
6. Debug and mature the GUI software to increase usability.
7. Port the GUI software to Visual C++ to increase reliability and performance.

5.5 SPOTR Output

The output of the SPOTR is highly programmable depending upon application requirements. Available outputs include crosshair overlay on the input RS-170 video, postprocessor results text file of a mission stored on disk and displayed on the GUI display upon request, and captured correlation planes. The video overlay and text file outputs are created while maintaining 800 Hz correlation. The GUI or text editor analysis of the postprocessor results is an off-line and nonreal-time process. The captured correlation plane requires considerable CPU and bus activity which slows the process down to approximately 10 Hz.

5.6 SPOTR Documentation

There are several pieces of documentation in addition to the Final Report that describe the various features and operations of the SPOTR. These documents include the SPOTR Users Manual, the SPOTR Interface Control Document, the Optical Alignment Procedure, and the set of SPOTR Engineering Drawings. The User Manual, ICD and alignment procedure are included as appendices to the Final Report.

6.0 Processor Testing

The TOPS program was designed with a fairly extensive set of testing throughout the program life cycle. These tests range from imagery collections to component and vendor acceptance testing to the final captive carry flight testing conducted at Redstone Arsenal, AL. Included were a large number of firsts for the optical pattern recognition community including systematic environmental testing of key components and two fully programmable optical processing systems and the extensive field testing of the processors. The complete list of tests conducted and documented are listed below.

Preliminary Tank Turntable Data Collection
U.S. Army MICOM Redstone, AL October 8-10, 1991

Captive Carry I Data Collection
U.S. Army MICOM, Redstone, AL March 4, 1992

Final Tank Turntable Data Collection
U.S. Army MICOM, Redstone, AL March 16-17 1992

Captive Carry II Data Collection
U.S. Army MICOM, Redstone, AL September 14-24, 1992

RT6 CCU Performance Evaluation
Photonic Systems Center, Waterton, CO. July-December 1992

RT6-E Component Environmental Evaluation

EMF and AVL, Waterton, CO. December 1992

Flyable Prototype Environmental Evaluation
EMF and AVL, Waterton, CO. January 1994.

SPOTR Acceptance Testing
Redstone Arsenal, AL. July 1994

SPOTR Tower Test
Redstone Arsenal, AL. July-August 1994

SPOTR Captive Carry Test.
Redstone Arsenal, AL. August 1994

Operational Test Set (OTS)

Table 6.0-1. Images and Filters in OTS.

	Start	End	Image ID	Filter	Filter Name	Peak Location	FOM
1	1	30	bigx.fly	0	bigx.flf	(64,64)	
2	31	60	bigo.fly	1	bigo.flf	(64,64)	
3	61	90	xoin_c.fly	2,3	x_c.flf, o_c.flf	(72,72) (56,56) (56,72) (72,56)	
4	91	120	xoin_e.fly	2,3	x_c.flf, o_c.flf	(10,10) (10,64) (118,64) (118,118)	
5	121	150	trbin.fly	4,6	trbin.flf	(64,64)	
6	151	180	trsob.fly	5	trsob.flf	(64,64)	
7	181	210	trb_b.fly	4,6	trbin.flf	(64,64)	
8	211	240	trs_b.fly	5	trsob.flf	(64,64)	
9	241	270	trb_n1.fly	4,6	trbin.flf	(64,64)	
10	271	300	trbn2.fly	4,6	trbin.flf	(64,64)	
11	301	330	f4_1.fly	7	f4r_.flf	(105, 105)	
12	331	360	f4_2.fly	7	f4r_.flf	(100, 100)	
13	361	390	f4_3.fly	7	f4r_.flf	(90,90)	
14	391	420	f4_4.fly	7	f4r_.flf	(80,80)	
15	421	450	f4_5.fly	7	f4r_.flf	(70,70)	
16	451	480	f4_6.fly	7	f4r_.flf	(60,60)	
17	481	510	f4_7.fly	7	f4r_.flf	(60,50)	
18	511	540	f4_8.fly	7	f4r_.flf	(55,40)	
19	541	570	f4_9.fly	7	f4r_.flf	(50,30)	
20	571	600	f4_10.fly	7	f4r_.flf	(50,20)	
21	601	630	f4_11.fly	7	f4r_.flf	(50,10)	
22	631	660	hin1.fly	8	hash0.flf	(22,21) (64,63)	
23	661	690	hin2.fly	9	hash 22_5.flf	(64,64) (64,22)	
24	691	720	hin3.fly	10	hash45.flf	(64,64) (105,22)	
25	721	750	hin4.fly	11	hash090.flf	(106,63) (64,64)	
26	751	780	hin5.fly	12	hash1575.flf	(105,105) (64,64)	
27	781	810	hin6.fly	13	hash135.flf	(64,64) (64,105)	
28	811	840	hin7.fly	14	hash1125.flf	(64,64) (22.105)	
29	841	870	T-72_1.fly	15	simple		
30	871	900	T-72_1.fly	16	simple		
31	901	930	T-72_1.fly	17	simple		
32	931	960	T-72_1.fly	18	simple		
33	961	990	19932.fly	19	simple		
34	991	1020	19933.fly	20	simple		
35	1021	1050	19934.fly	21	simple		
36	1051	1080	19935.fly	22	simple		

Throughout the system-level testing a standard set of images and filters were used to assess correlation performance. This set of data has been defined as the operational test set (OTS) and is described in Table 6.0-1. The purpose of the OTS is to provide a standard set of correlation tests that can be used to conduct performance baselines and health monitoring.

The OTS was used during the processor environmental testing to test operational performance and to assess the configuration of the processor after testing. During the final field testing at Redstone Arsenal the OTS was used at the beginning and end of each day to assess processor performance and was used during troubleshooting and performance optimization efforts.

Determination of performance parameters

The initial performance indication used was the quick look test analysis which is based on the presence or absence of the Target Indication Crosshair (TIC) overlaid on the video output which has bee termed the correlator results video (CRV). Real time visual monitoring of the CRV verifies that the OPM is correlating but a frame by frame examination during the post test analysis is required to derive quantitative information. This is achieved with the use of a text file of results provided by the postprocessor which has been termed the correlator results data (CRD).

The real time video presents the first indication that the SPOTR has met performance requirements. A TIC is shown on the output video monitor every time the SPOTR determines that the target is in the field of view. The "Quick Look" test analysis consists of single framing through the CRV and confirming visually the presence and location of the TIC.

Additional detail is included in the correlator results data (CRD) report. The OTS images and filters are numbered sequentially. Their combined performance is documented in the CRD. During OTS tests, the input #, filter #. the x/y location, delay time and FOM for each correlation is output from the postprocessor as the CRD. Described in the following paragraphs is the key operating information that is output.

Each time the SPOTR detects a correlation peak, a CRD is generated by the post-processor hardware and stored in the SPOTR. This report contains the following information concerning the detected correlation(s):

Delay Time	The results of an internal timer that starts when the frame is presented to the input SLM and stops when the crosshair is overlaid on that frame.
Peak Location	The X and Y coordinates of the correlation peak with respect to the 128 x 128 pixel resolution of the detector array.
Input #	A numerical ID indicating the frame number of the input image supplied by the preprocessor for which the correlation was found. This number is reset to zero at the "start" of a search operation.
Filter #	A numerical ID indicating the particular filter from which the CRD was generated.
Horner	A laser intensity value assigned to the filter that has been previously determined to give the best response for that filter.
Figure of Merit(FOM)	A measure of the quality of the correlation between a filter and a potential target of interest. It is based on the multiplication and summation of the correlation peak values and the elements of a convolution kernel defined in the postprocessor. A threshold will be applied to the FOM to determine whether a TIC and report are made in the CRV and CRD respectively.

Figure 6.0-1 illustrates how the parameters are reported in the CRD. The overall performance of the SPOTR is affected by both hardware and software response, by the selected modes of operation, and by the amount of correlation data being processed. The delay time is used to quantify these timing effects. Probability of Recognition(Pr), False Alarm Number(FAN) and Location Accuracy(LA) are determined by analyzing the results for each input frame.

input image: 2.inp time-of-day: 18:04:34.02

Delay	fom	x	y	input#	filter#	horner
30650	140	66	62	2	1	0025
30700	125	66	63	2	1	0025

---

input image: 3.inp time-of-day: 18:04:34.35

Delay	fom	x	y	input	filter#	horner
40600	140	66	62	2	1	0038
40650	125	66	63	2	1	0038
40700	140	66	62	2	1	0038
44750	125	66	63	2	1	0038
50550	140	66	62	2	1	0038
50600	125	66	63	2	1	0038
50600	140	66	62	2	1	0038
50700	125	66	63	2	1	0038
50700	140	66	62	2	1	0038
50750	125	66	63	2	1	0038

Figure 6.0-1. Example of Correlator Results Data (CRD).

Performance Definitions

The CRD is used to determine performance information of Latency (Lt), Throughput (Tp), Location Accuracy (LA), Probability of recognition (Pr) and False Alarm Number (FAN).

Latency (Lt)

The Lt of the SPOTR is defined as the delay time between sensor input to the SPOTR and the Correlator Results Data output for any particular input frame. The Lt goal in search mode is 1.14 sec. The Lt goal in track mode is 0.14 sec.

Throughput (Tp)

The Tp of the SPOTR is defined as the rate at which the SPOTR processes video frames. The SPOTR update rate goal is 0.88 Hz in Search Mode and 5.3 Hz in track mode.

Location Accuracy (LA)

LA is the accuracy with which the SPOTR locates the correlation peak. The SPOTR Location Accuracy goal is ±7 pixels..

Probability of Recognition (Pr)

The Pr is defined as the probability of recognizing a target that is in clear view of the sensor unobstructed by weather, terrain, vegetation, or camouflage netting. The Pr goal of the SPOTR during our field testing is 90%.

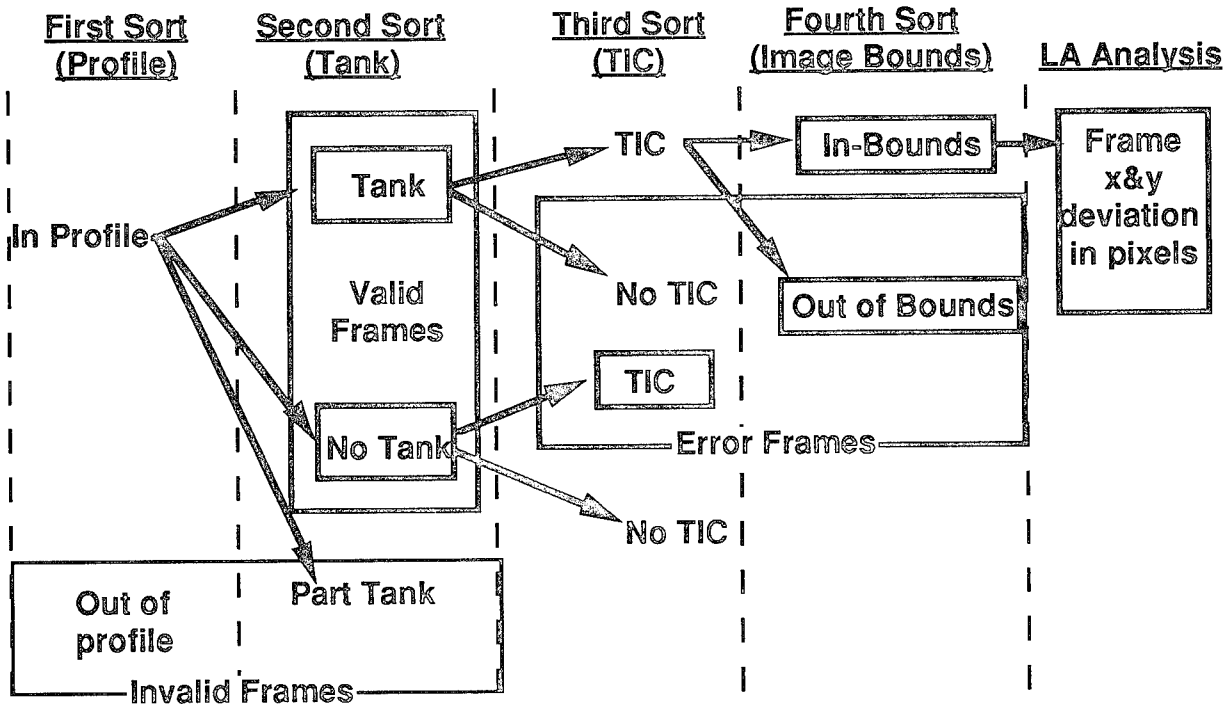
False Alarm Number (FAN)

The FAN is defined as the number of TICs reported which have location positions outside the target boundaries per frame of input video. The FAN goal of the SPOTR is less than 0.05 per frame when the Pr is 90% (This number corresponds to a 90% certainty that no two false alarms will occur within 2.7 sec of each other).

Post Test Performance Analysis

A more detailed post test performance analysis was conducted on a select set of tests and provides a more thorough statistical analysis of the SPOTR performance. The steps in conducting this analysis are highlighted below and illustrated in Figure 6.0-2.

1. Sort the Correlator Results Video(CRV) frame by frame for In Profile frames
2. Sort the Correlator Results Video(CRV) frame by frame for a listing of valid frames
3. Sort the valid frames for the listing of TIC frames.
4. Sort the TIC frames for the listing of Error Frames.
5. Determine the total number of framed processed.
7. Probability of Recognition(Pr) is then determined by dividing Item 1. by Item 5.
8. False Alarm Number(FAN) is then determined by dividing Item 3. by Item 5.
9. Location Accuracy(LA) will be determined by selecting frames that have a cross-hair overlay and comparing the cross-hair location with the centroid of the tank in that particular frame. Cut out tank, determine centroid and compare with the cross-hair location after factoring in the previously determined bias of the filter centroid.



$$Pr = \frac{(\text{In Profile, All Tank, TIC, In-Bounds})}{(\text{All Tank})}$$

$$FAN = \frac{(\text{In Profile, All Tank, TIC, Out of Bounds}) + (\text{In Profile, no Tank, TIC})}{(\text{Valid Frames})}$$

$$\text{LA average} = \frac{\sqrt{F1xdev^2 + F1ydev^2} + \ldots \sqrt{F_n xdev^2 + F_n ydev^2}}{}$$

Figure 6.0-2. Post Test Performance Analysis Approach.

6.1 Component Testing

The optical, electro-optical components and electrical subassemblies for the Flyable Prototype and SPOTR optical processors were specified to meet a variety of performance and configuration requirements when procured. These specifications were verified when each items was received. All the components in both processing systems satisfy the component requirements except for the FLC SLMs. We had specified a $\lambda/4$ flatness requirement across the active area of the SLMs. This requirement was not met for the integrated and spare components for the systems. Flatness was measured in an interferometer but based on the configuration of the SLM it is very difficult to measure the flatness of the VLSI backplane and thus the flatness was not verified. Most of the SLMs received had a front surface flatness of less than $3\lambda/4$. This performance was analyzed in the context of Fourier transform and correlation performance and was determined to be acceptable for the required system performance.

6.2 Environmental Testing

Vibration Testing

To ensure that the Flyable and SPOTR optical processor designs were able to support operation under the UH-1 environments in Huntsville, AL we conducted a series of acceleration and thermal tests on several critical electro-optic components and the complete processing systems. Shock was not rigorously considered in the design and analysis. The approach to shock is to use special handling precaution when moving the processor and to not subject the integrated system to excessive levels in the field testing.

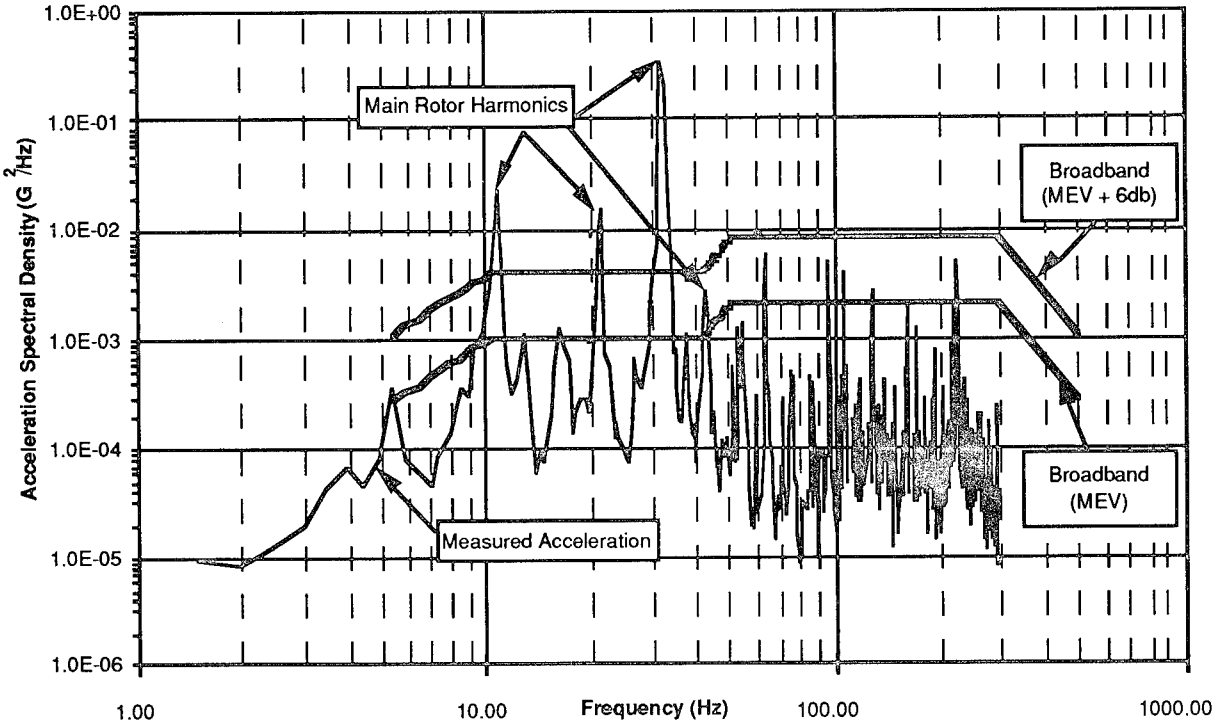


Figure 6.2-1. UH-1 Vibration Power Spectra, MEV, and MEV+6dB Envelopes.

The test philosophy was modified from practices developed from considerable heritage in developing flight and space qualified systems. The Flyable Prototype was designed, developed and tested to qualify the design for our target environment. The SPOTR which is a single protoflight, deliverable piece of hardware was tested to lower acceptance levels. The qualification vibration levels were determined by first measuring the actuals based on the average of several captive carry flights during an imagery collection. A margin envelope of 6dB above the measured average was used for the Flyable Prototype qualification testing. The SPOTR acceptance testing was conducted at the average measured levels called the maximum expected value (MEV). Figure 6.2-1 illustrates the UH-1 MEV and MEV+6dB levels of vibration which were applied to the SPOTR and Flyable Prototype, respectively, in the X and Z axes during testing. The systems were operated while under the environments for periods of 30 seconds to 10 minutes. The performance was analyzed on a per correlation basis at correlation rates of up to 800 Hz and visual observations of the correlation plane intensity distribution were made at much slower rates.

As reported in detail, during the several days of testing there were no correlation anomalies or losses in performance observed. On two occasions, one each with the Flyable and SPOTR there was a hard disk access error. These errors occurred when the system was being vibrated in an axis normal to the disk. These errors were not fatal and are not consistent with normal processor operation as all operations are conducted in RAM during a mission. Hard disk usage is

used in post test archival of results and analysis. These single event anomalies were analyzed to occur with a probability of less than 0.25% and were not mission critical so we qualified the designed and accepted the SPOTR in both cases.

During the field testing at Redstone Arsenal both processors were integrated and flown in the UH-1. There was no observed performance degradation due to the vibration environments in nearly 30 hours of flight testing at a 500 Hz correlation rate.

Thermal Testing

The operational performance of the Flyable and SPOTR system was also evaluated over a series of thermal cycles ranging from 48 to 108°F. The result of the testing indicated no significant thermal sensitivity over the operational range. The only recognizable degradation in performance occurred when the system temperature changed from 48° to 76°F at rates of 4°F per minute. This rapid temperature rise from a cold temperature resulted in the loss of some contrast in the SLM with a corresponding yet lesser effect on overall correlation performance. Since the completion of the TOPS testing this phenomena has been repeated in other devices with the effects being more prominent and perhaps permanent when the storage temperature was lowered to levels around 30°F. Subsequent efforts to recondition the SLM have been unsuccessful from 30° whereas we had success from 48°F. This represents a concern with the FLC SLM which deserves additional attention. Measures can be taken to condition the SLM thermal environment with a variety of conventional techniques however they require additional power and volume and add weight to the system.

The TOPS field testing was conducted in Redstone Arsenal, AL during July and August in which the temperature range varied from the mid 60°s to mid 90°s. The processors performed very well over the entire temperature range. The only adjustments made over the temperature extreme were slight rotations to the half wave retarders to adjust the system throughput. This is likely to be necessitated by changes in the amount of FLC molecular rotation as a function of temperature which changes the amount of polarization rotation and the efficiency effects associated with the polarizing beam splitters. This might be explained by changes in FLC viscosity.

Humidity

There were no formal humidity tests conducted on the Flyable or SPOTR processors. Our approach was to design the SPOTR to be robust to humidity by creating a sealed and conditioned optical subsystem. The SPOTR was designed with an O-ring seal and desiccant cartridge/humidity indicator system to prevent humidity from being persistent in the subsystem in non-condensing environments of up to 98% at less than 10,000' above sea level.

The TOPS field testing was conducted under humidity environments that approached 100%. There was no observable performance degradation over the course of 4 weeks that the processor was integrated into the UH-1 cargo bay. Of particular interest was that the Flyable Prototype, which was not designed with the features to minimize humidity, was the primary processor used during the captive carry demonstrations where the maximum humidity environments were realized.

6.3 Tower Testing

The objective of the Tower Test is to evaluate the M60A2 recognition performance of the SPOTR while operating with live input images from the RSS seeker without the UH-1 helicopter environment and its logistical constraints. The test covered as much of the FOG-M missile profile as is physically possible from the Redstone Arsenal, Robert F. Russell Measurement Facility Tower. The tower test was conducted during the month of July 1994. The tower test is broken into a series of three tests which evaluate the SPOTR azimuth, elevation, and scale invariance and its ability to discriminate the target from non-targets.

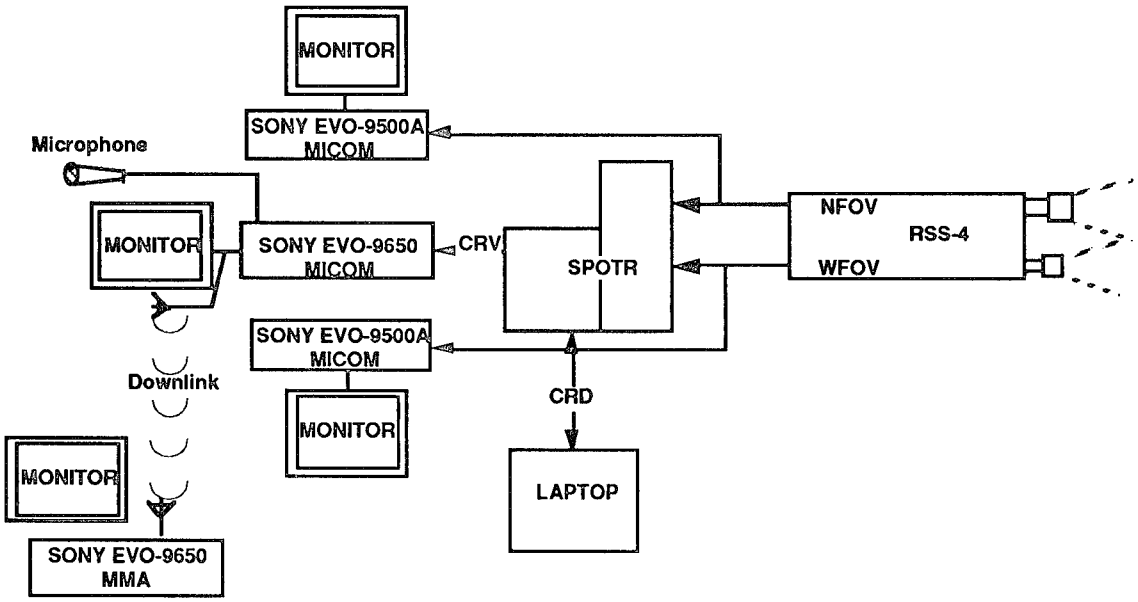


Figure 6.3-1. Tower and Captive Carry Rack Block Diagram.

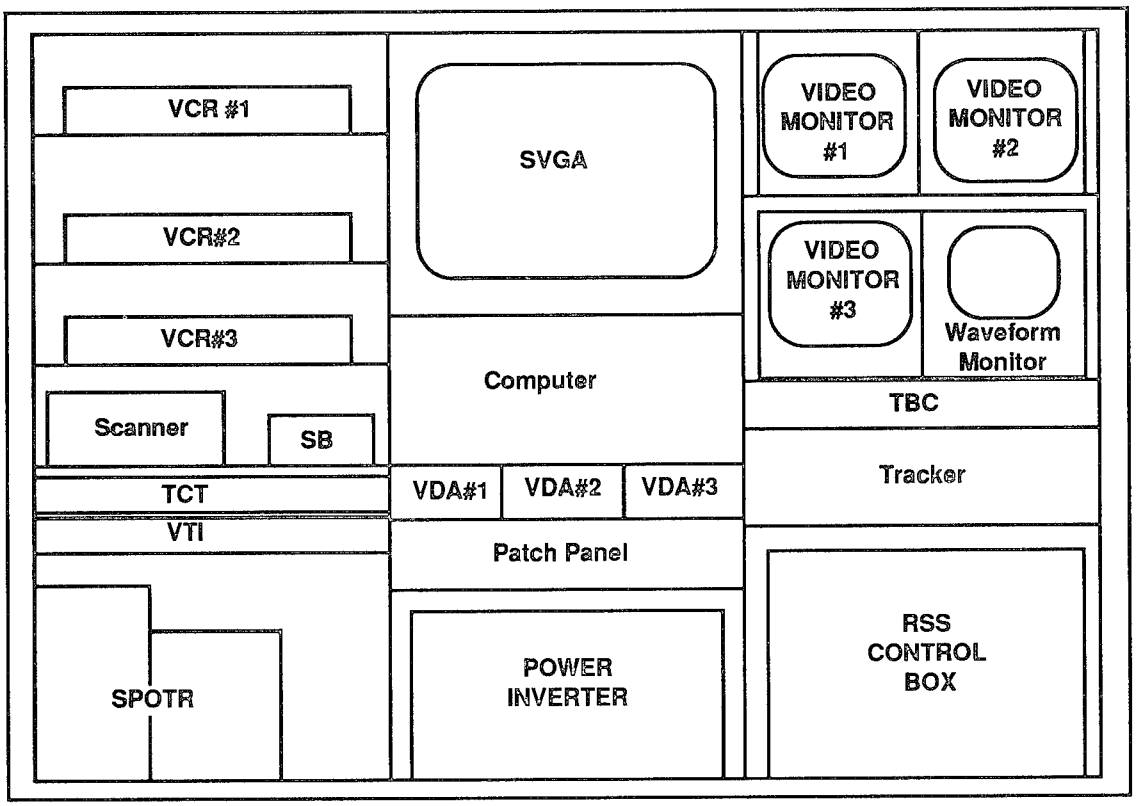


Figure 6.3-2. Tower and Flight Rack Equipment Layout.

The tower test was conducted from the elevator of the Measurement Facility Tower. The elevator in the tower housed the test equipment so that the various look angles and ranges to target could be simulated by moving up and down in the elevator while driving the M60A2. Figures 6.3-1 and 6.3-2 illustrate the test configuration used in both the Tower and Flight testing.

As illustrated in Figure 6.3-3, two separate locations around the tower were used to enable ranges to the target from 200m to 700m to be used in the three series of tests. These two locations represented extremes in the target recognition problem from many pixels on target with little clutter and high contrast to few pixels on target with moderate clutter and very poor contrast.

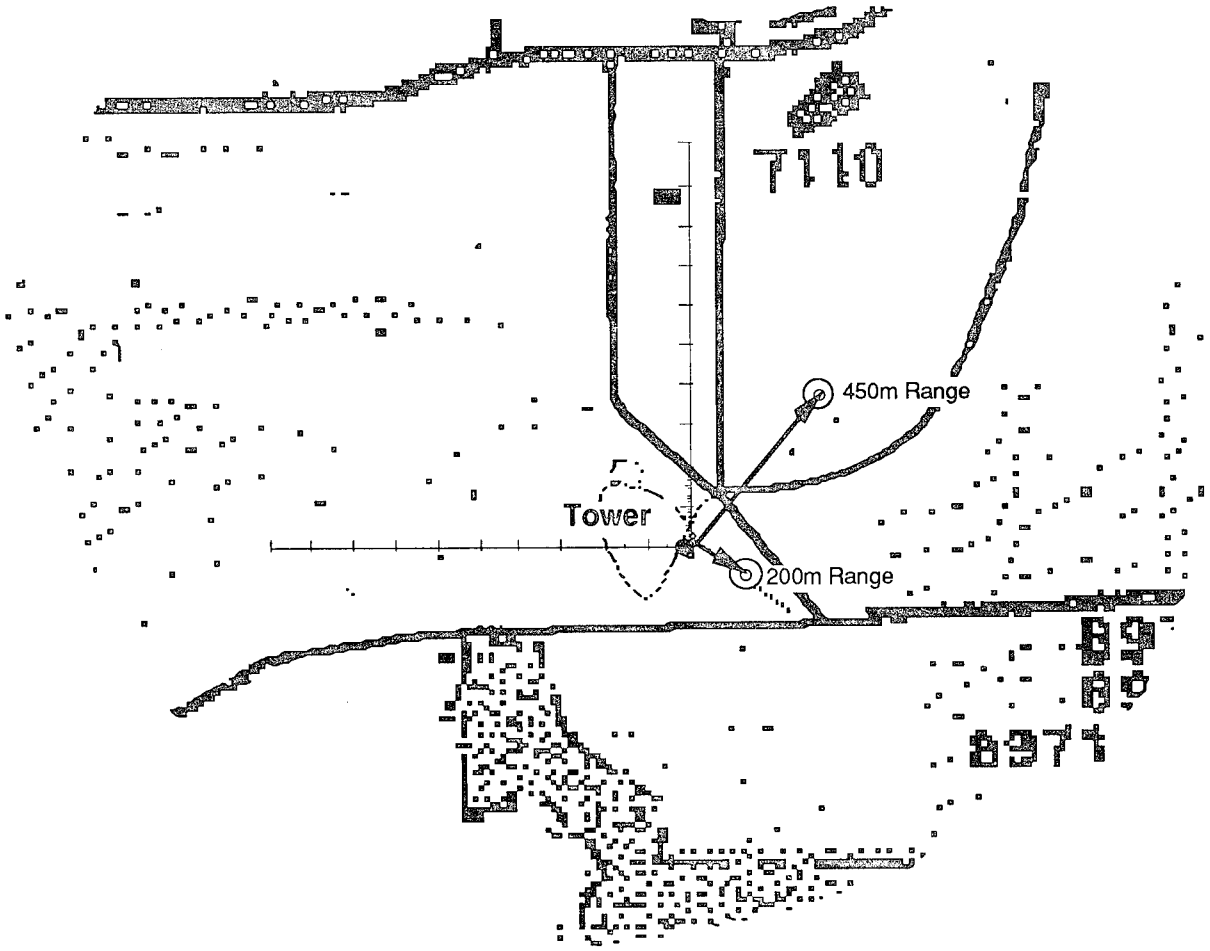


Figure 6.3-3 Tower Test Area Layout.

Target Aspect Possibilities Available From Tower Facility

Table 6.3-1 defines the sensor look angles and ranges that can be provided from each elevator floor. This table was used often to determine possible target locations and elevator floor configurations to emulate various aspects of the captive carry field testing.

Table 6.3-1. Slant Ranges and Elevation Angles Available from Tower.

Elevator Level	each Level Meters	Slant Range@ 6° m	Slant Range@ 7° m	Slant Range@ 8° m	Slant Range@ 9° m	Slant Range@ 10° m	Slant Range@ 11° m	Slant Range@ 12° m
7+	21.0	200.0	171.2	149.6	132.7	119.2	108.1	98.9
8	22.7	216.0	184.9	161.6	143.4	128.8	116.8	106.8
9	25.8	245.0	209.8	183.3	162.6	146.1	132.5	121.2
10	28.8	274.0	234.6	204.9	181.9	163.4	148.2	135.5
11	31.9	303.0	259.4	226.6	201.1	180.6	163.9	149.8
12	34.9	332.0	284.2	248.3	220.3	197.9	179.5	164.2
13	37.9	361.0	309.1	270.0	239.6	215.2	195.2	178.5
14	41.0	390.0	333.9	291.7	258.8	232.5	210.9	192.9
15	44.0	419.0	358.7	313.4	278.1	249.8	226.6	207.2
16	47.1	448.0	383.5	335.1	297.3	267.1	242.3	221.5
17	50.1	477.0	408.4	356.8	316.6	284.4	257.9	235.9
18	53.2	506.0	433.2	378.4	335.8	301.6	273.6	250.2
19	56.2	535.0	458.0	400.1	355.1	318.9	289.3	264.6
20	59.3	564.0	482.8	421.8	374.3	336.2	305.0	278.9
21	62.3	593.0	507.7	443.5	393.5	353.5	320.7	293.2
22	65.4	622.0	532.5	465.2	412.8	370.8	336.3	307.6
23	68.4	651.0	557.3	486.9	432.0	388.1	352.0	321.9
24	71.5	680.0	582.1	508.6	451.3	405.4	367.7	336.3
25	74.5	709.0	606.9	530.3	470.5	422.6	383.4	350.6
26	77.6	738.0	631.8	552.0	489.8	439.9	399.1	364.9
27	80.6	767.0	656.6	573.6	509.0	457.2	414.8	379.3
28	83.7	796.0	681.4	595.3	528.3	474.5	430.4	393.6
27	86.7	825.0	706.2	617.0	547.5	491.8	446.1	408.0
30	89.8	854.0	731.1	638.7	566.7	509.1	461.8	422.3
31	92.8	883.0	755.9	660.4	586.0	526.4	477.5	436.6

Target Array

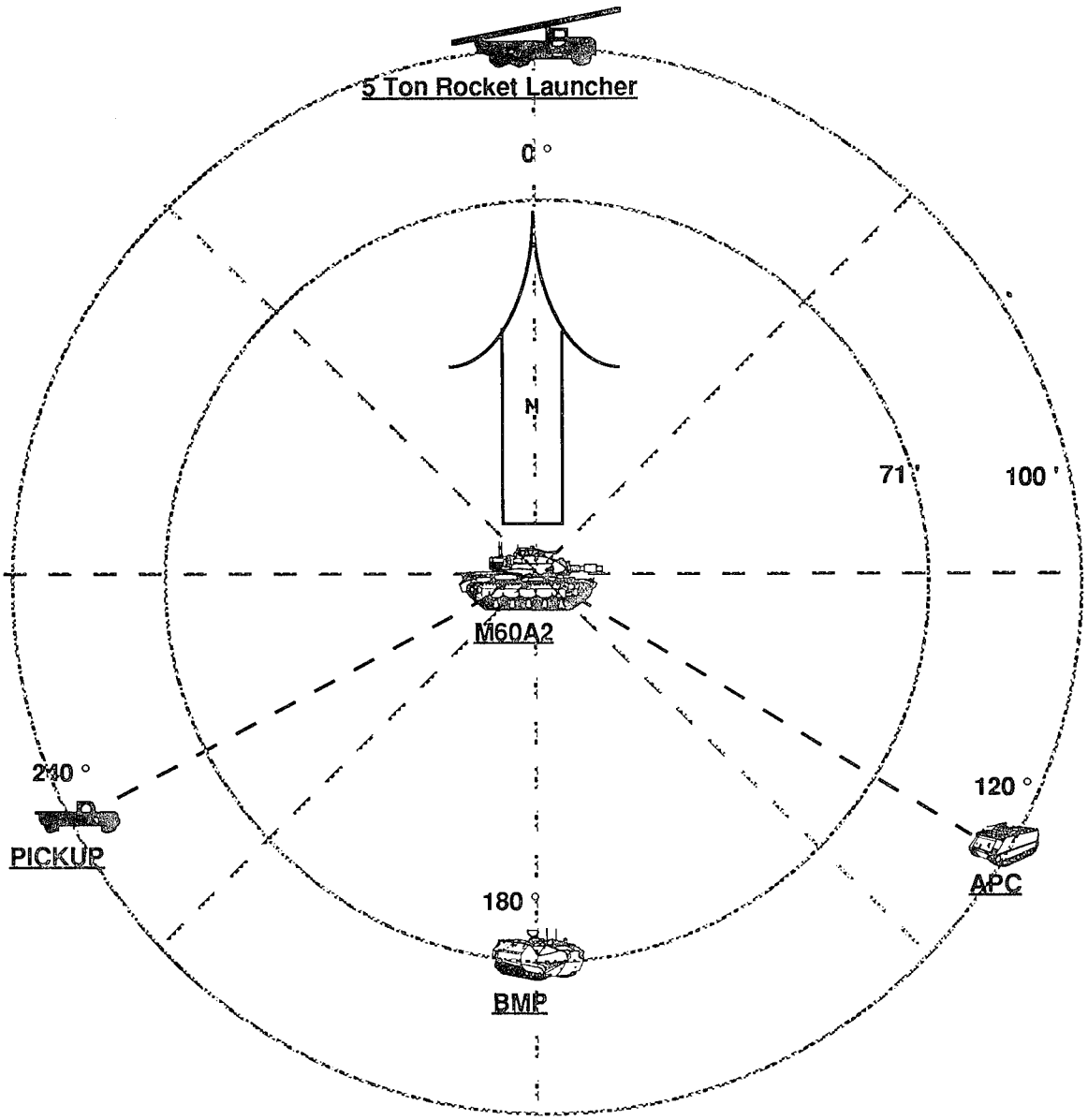


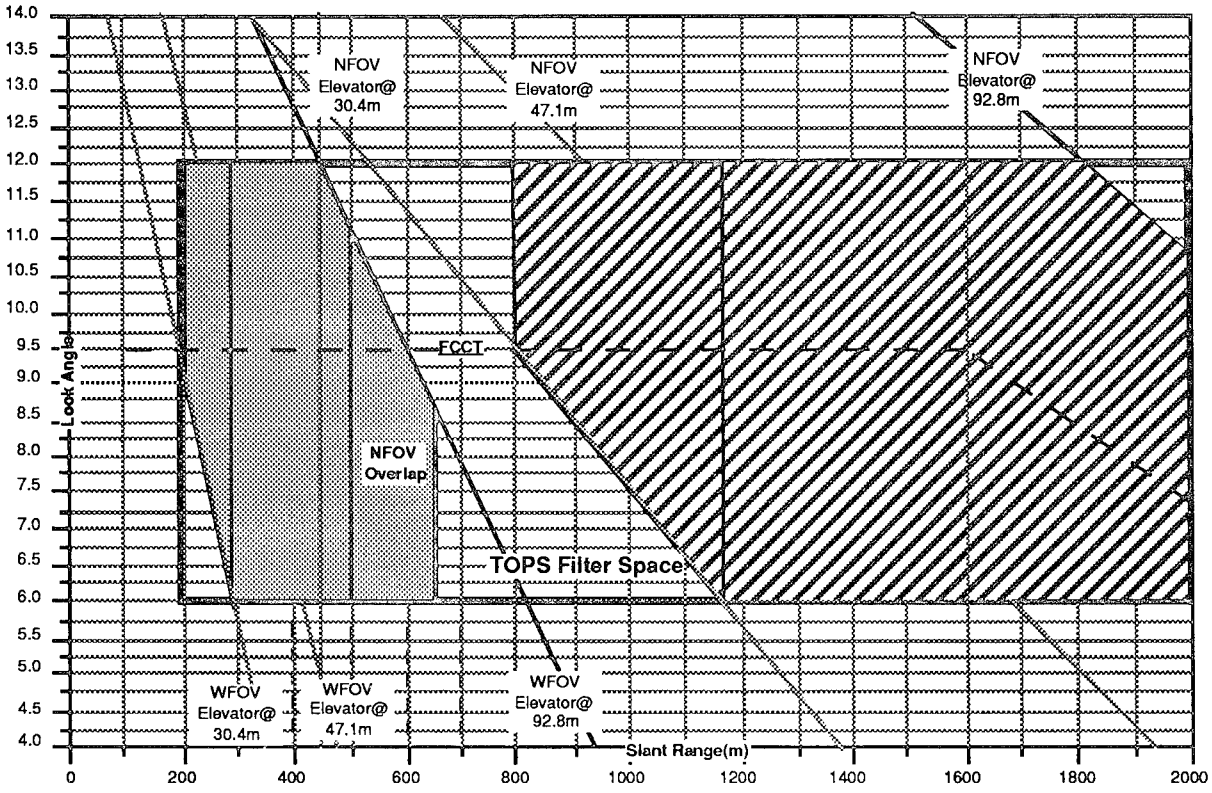
Figure 6.3-4. Tower and Flight Test Basic Target Array Layout.

Figure 6.3-4 illustrates the target array used for a portion of the tower test and in all of the captive carry testing. This is the same target array as used in the previous captive carry imagery collections. The target array allows for several nontargets to be within both RSS fields of view over much of the testing while also ensuring that the M60A2 is not occluded by another nontarget.

Tower Test Sequence

Table 6.3-2. Tower Test Sequence Summary.

TEST	TARGET LOOK AZIMUTH	TARGET LOOK ELEVATION	FLIGHT PATH	NON TARGET	SLANT RANGE M	RANGE LOCATION
Series 1 Test1A	270°	6°-12°			200	200m Tower Road
Series 1 Test1B	0°-360°	9°			200	200m Tower Road
Series 1 Test2A	270°	6°-12°			250	200m Tower Road
Series 1 Test2B	0°-360°	9°			250	200m Tower Road
Series 1 Test3A	270°	6°-12°			300	200m Tower Road
Series 1 Test3B	0°-360°	9°			300	200m Tower Road
Series 2 Test1A	270°	6°-12°		A113	200	200m Tower Road
Series 2 Test1B	0°-360°	9°		A113	200	200m Tower Road
Series 2 Test2A	270°	6°-12°		A113	250	200m Tower Road
Series 2 Test2B	0°-360°	9°		A113	250	200m Tower Road
Series 2 Test3A	270°	6°-12°		A113	300	200m Tower Road
Series 2 Test3B	0°-360°	9°		A113	300	200m Tower Road
Series 3 Test 1A	90°	6°-12°		CCII(ALL)	450	450m Thiokol
Series 3 Test 1B	0°-360°	9°		CCII(ALL)	450	450m Thiokol
Series 3 Test 2A	90°	6°-12°		CCII(ALL)	550	450m Thiokol
Series 3 Test 2B	0°-360°	9°		CCII(ALL)	550	450m Thiokol
Series 3 Test 3A	90°	6°-12°		CCII(ALL)	650	450m Thiokol
Series 3 Test 3B	0°-360°	9°		CCII(ALL)	650	450m Thiokol



Test Series 1-Target Tank on Tower Road @ 200m to 300m Rotating all azimuths

Test Series 2-Target Layout Center at 450m and M60A2 Target Tank is Driven + 200 and -150m from Center

WFOV Actual Filter Space Covered By 8° FOV From Tower Elevator @ 30.4m to 92.8m

NFOV Apparent Filter Space Covered By 8° FOV From Tower Elevator @ 30.4m to 92.8m

Figure 6.3-5. Tower Test Composite (Series 1-3) Constraints.

As illustrated in Table 6.3-2 the Tower Test was broken into three series of tests. The first series of tests were at short ranges and include only the M60A2 tank at the 200m site. These tests serve the purpose of a fundamental checkout of the SPOTR, RSS and data acquisition interfaces as well as the basic performance of the ATR algorithms. The second series of tests were an abbreviated version of the first set with the addition of a nontarget (A113 APC) to test the discrimination performance of the ATR algorithms. The third series of tests were conducted at an extended range from the 700m site, with more clutter, lower contrast and with the complete target array as illustrated in Figure 6.3-4. The third series of tests most closely matches the conditions of the captive carry flight as accurately as possible from the Tower Facility. Figure 6.3-5 shows how the combined series of three sets of tests covers a large portion of the available filter space and expected captive carry flight profile (FCCT). Ideally, there would be shaded areas (dots or diagonal lines) covering the full extent of the dotted FCCT line. This would indicate the ability to emulate from the tower any potential ATR task that might be encountered while flying the helicopter tests. The plot in Figure 6.3-5 indicates less than full coverage with the two sensor fields of view.

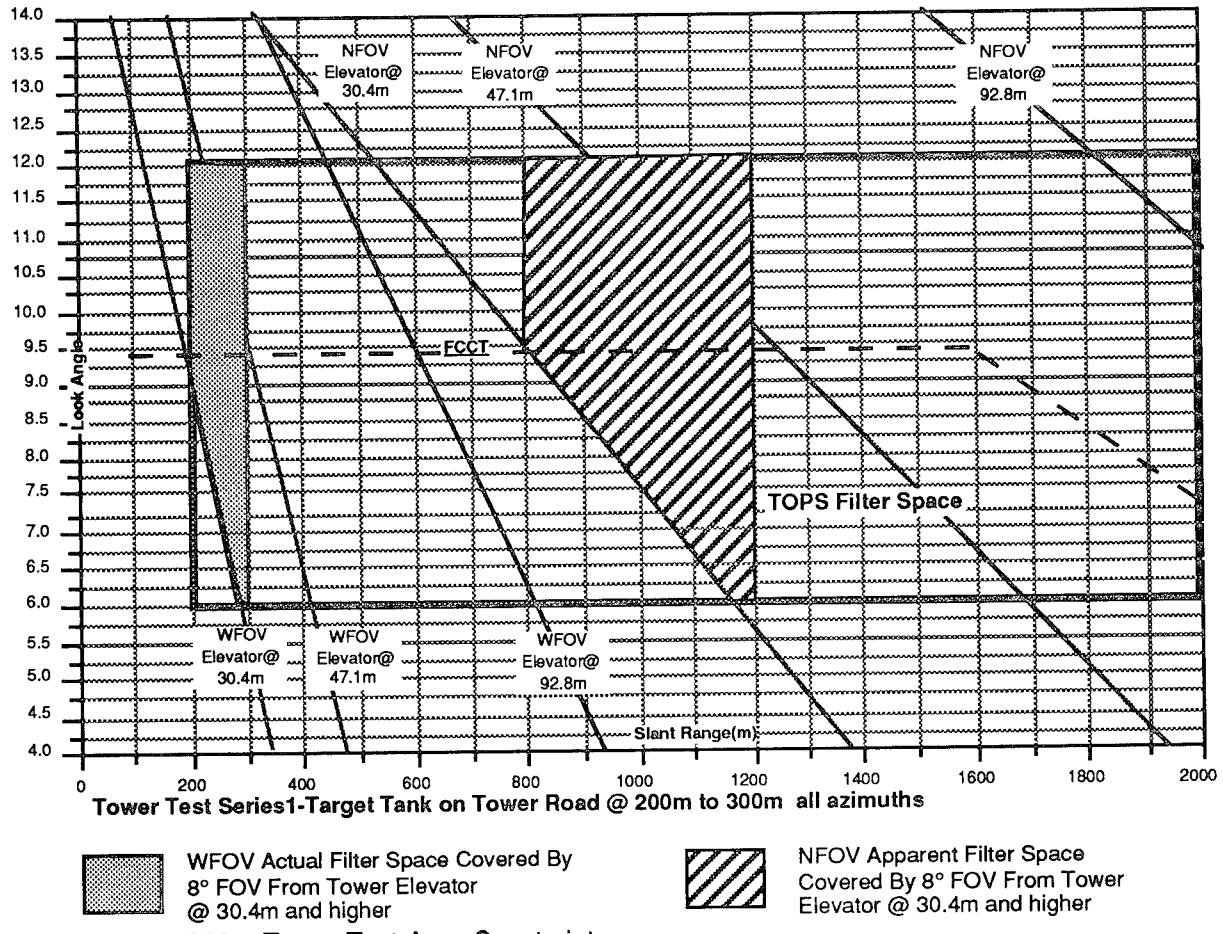


Figure 6.3-6. 200m Tower Test Area Constraints.

Test series 1 and 2 were conducted on the tower road within the TSMF at a range of 200 to 300m with the M60A2 alone and including the A113 APC respectively. Figure 6.3-6 depicts the physical constraints that can be achieved from the tower facility for the combined series 1 and 2 tests at the range bounded by the constraints of the height of the tower, the filters developed, the field of views of the RSS seeker, and the FOG-M missile profile.

The basic test configuration used for test series 1 & 2 is listed below.

Test Range: Tower Road, 200 meter Range
Sensor (Elevator) Height: 21m to 62m
Target(M60A2) Motion: 200m to 308m, Stationary, Moving and Rotations
Look Angle: <6° to >12°
Non Targets: A113, Pickup Truck
Azimuth: 0° to 359.9°
Filters Required: All TOPS, OTS
Test Criteria: See Table 2
Target Configuration: Barrel +10° elevation, Turret-0°(Barrel Forward)
VCR #1: WFOV RSS
VCR #2: NFOV RSS
VCR #3: SPOTR Output (CRV)

The test procedure sequence used in performing test series 1 and 2 was similar to the example given below.

Tower Test Series 1 Test 1

A1. Start conditions
   a. Target Position: 200m stake, tower road
   b. Target Look Azimuth: 270° (full broadside, left)
   c. Start Elevator 6°Position: Level 7 + 4 ft(21m)
      Elevator 12°Position: Level 15 (44m)
      Elevator 9°Position: Level 11(31m)
   d. Non Targets: None
   e. WFOV
2. Perform OTS test and determine that the operation of the SPOTR is within baseline
3. Start VCR#1 and #3
4. Start the SPOTR in search mode and confirm operation by "Quick Look"
5. Raise elevator to 12° position while operating SPOTR and recording CRV and CRD
6. Perform "Quick Look" to determine if 1-5 must be repeated or proceed to next step
7. Repeat step 3 through 6 while lowering elevator to 9° level

B8. Repeat step 3 &4 while driving target tank clockwise in a 10m dia. circle

9. Perform post test analysis

Tower Test Series 3 (450m Tower Test Range)

Test series 3 was conducted on the Thiokol Area with the complete target array as defined in Figure 6.2-4 at ranges of 450 to 600m from the Tower Facility. Test series 3 was designed to test the SPOTR target detection and discrimination performance under conditions similar to the final captive carry test. Figure 6.3- 7 depicts the physical constraints that can be achieved from the tower facility at the ranges bounded by the constraints of the height of the tower, the filters developed, the field of views of the RSS seeker, and the FOG-M missile profile.

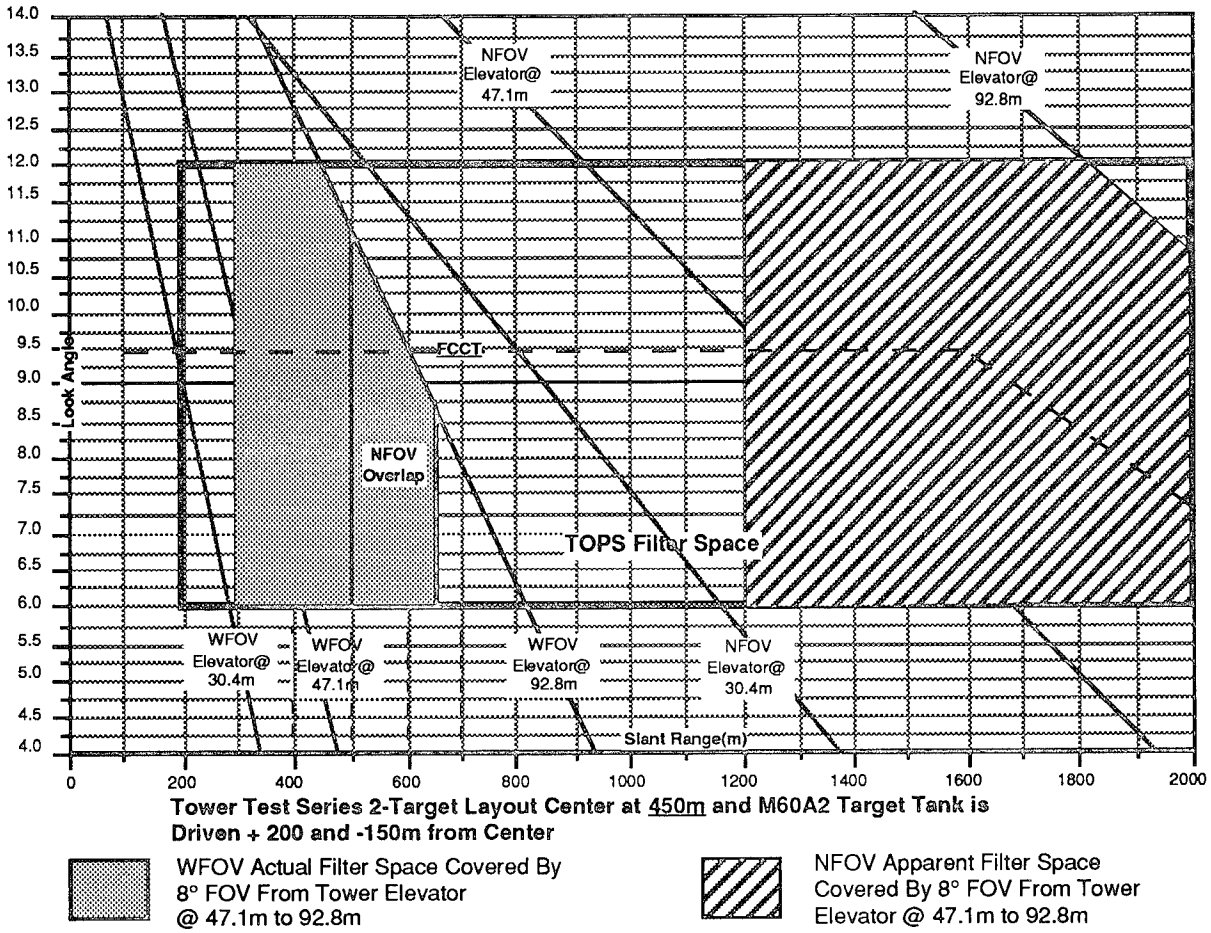


Figure 6.3-7. 450m Thiokol Area Tower Test Range Constraints.

The basic test configuration used for test series 3 is summarized below.

Test Range: Thiokol Area, 450 meter
Sensor (Elevator) Height: 47.1 to 92.8m
Look Angle: <6° to >12°(limited after 450m)
Target(M60A2) Motion: 4500m to 650m, circling and bisecting the CCII basic target layout. The final range capability and target motion may be limited by the tree height between the tower and the target location.
Non Targets: A113, BMP, 5 ton Truck with Rocket Launcher, Pickup Truck positioned the same as CCII (see diagram) and centered at 450m.
Azimuth: 0° to 359.9°
Filters Required: All TOPS & OTS

The test procedure sequence used in performing test series 3 was similar to the example given below.

Tower Test Series 3 Test 1

A1. Start conditions
a. Target Position: 450m stake, Thiokol Area
b. Target Look Azimuth: 90° (full broadside, right)
c. Start Elevator 6°Position: Level 16 (47m)

Elevator 12°Position: Level 31 (93m)
Elevator 9°Position: Level 24(71m)

d. Non Targets: ALL
e. WFOV

2. Perform OTS test and determine that the operation of the SPOTR is within baseline
3. Start VCR#1 and #3
4. Start the SPOTR in search mode and confirm operation by "Quick Look"
5. Raise elevator to 12° position while operating SPOTR and recording CRV and CRD
6. Perform "Quick Look" to determine if 1-5 must be repeated or proceed to next step
8. Repeat step 3 through 6 while lowering elevator to 9° level
B9. Repeat step 3 &4 while driving target tank clockwise in a 10m dia. circle
10. Perform post test analysis

Tower Test Results

The tower tests were the most informative and value-added tests conducted during the entire field testing in terms of optimizing the processor and sensor interface, associated operating software, and test procedures. The test period took longer than anticipated but was key to the flight testing success which were to come.

The sensitivity to light levels and the sensor inability to compensate was identified and minimized by appropriate modifications to the preprocessor. It was found that the performance of the sensor and processor were varied as a function of the time of day and from day to day. These variations are best explained by changes in lighting conditions and the resulting target to background contrast in the imagery being processed. The performance variations could be reduced by including a gain and level adjustment in the visible sensor or by transitioning to a seeker which is less sensitive to lighting conditions such as a FLIR, LADAR or radar. The filter management configuration item was improved tremendously including the ability to adjust parameters to vary probability of recognition and false alarm numbers, the addition of the reacquire and field of view switching schemes, and the use of multiple target aspect hypotheses in the initiation of track mode. The CRV was improved considerably by getting to a real-time cursor overlay which also changed in shape to signify search/reacquire or track modes of operation.

In test series 1 and 2 we learned that the elevation angle sensitivity of the system was not as severe as the azimuth sensitivity as moving the elevator even 5-10° outside of our designed elevation window of filters had little effect on performance for nominal depression angles of 9°. When driving the tank in a circle the system had a higher probability of detection when the tank was broadside than when it was end on. This is directly related to the number of pixels on target and how fast the target's binary signature varies as a function of azimuthal angles. The processor did an excellent job of discriminating the M60A2 from the A113 APC under all conditions in series 1 and 2.

In test series 3 we began to understand our range to target (pixels on target) and lighting condition sensitivities. It was found that the end on tank was more difficult to detect and track than the broadside representation for most ranges to target. However when there are an extremely large numbers of pixels on target the end on representation actually performed better. The conclusion is that a sufficient number of pixels on target must exist to achieve adequate target recognition performance. However when there are an excessive number of pixels on

target the differences in lighting conditions between filter references and field imagery becomes significant and can cause detection problems. The processor did a very good job of detecting and tracking the target in a fairly challenging set of background, contrast and clutter conditions. When the tank would drive too close to another vehicle their binary signatures would sometimes merge and cause detection problems but in general the processor performed very well under conditions similar to the final flight testing was anticipated to be.

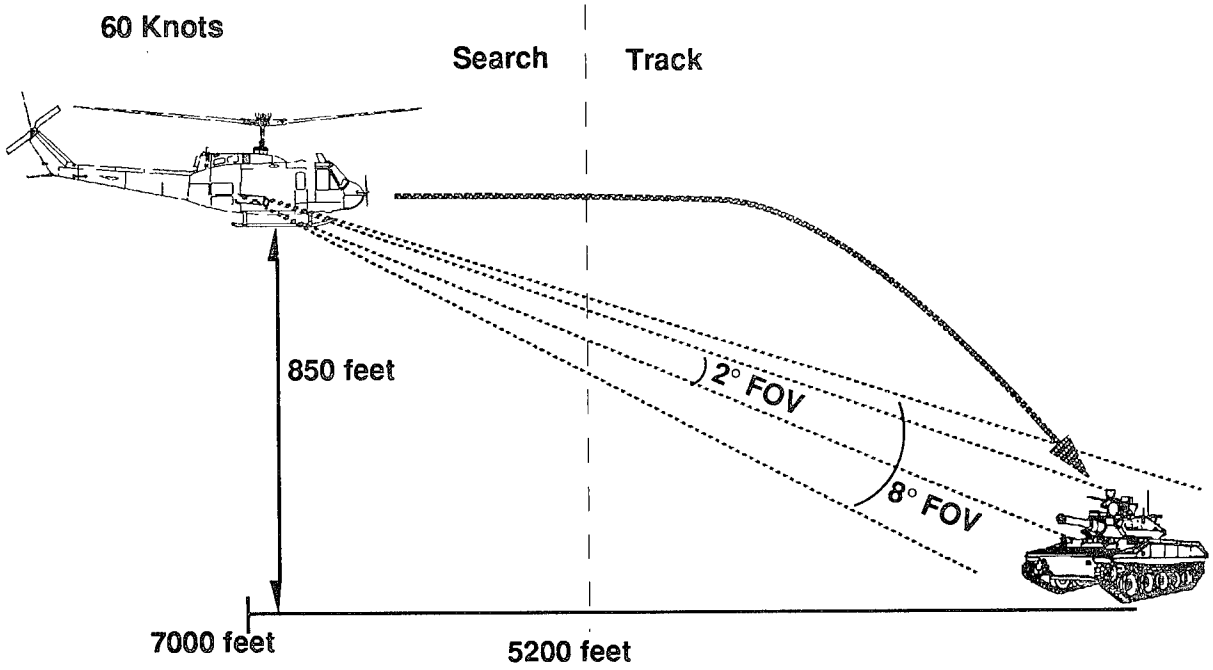
Demonstration Day Attendance

Three days of tower testing were dedicated for onsite visitation from interested parties. The captive carry demonstration was attended by approximately 40 people. Several attendees were on hand from various MICOM offices as well as many invited guests from around the country. The processor performed very well on the first and third days of the demonstration. The atmospheric visibility was extremely poor due to rain on the second day and resulted in intermittent processor performance. The seeker and processor were demonstrated to detect the target in the rain but performance was hampered by low light levels.

6.4 Captive Carry Flight Testing

The objective of the captive carry flight testing is to evaluate the pattern recognition performance of the optical processor with live input images from the RSS seeker while mounted in a UH-1 helicopter flying a flight profile similar to a Fiber optic Guided Missile (FOG-M). The captive carry flight testing was conducted at Redstone Arsenal, AL on Test Area 3. The testing occurred during the month of August 1994 over a four week period. Over one hundred flights were made against a target array that consisted of the M60A2 tank as the target and a variety of other tanks and other tracked vehicles used as clutter challenges for the pattern recognition system. In post test analysis 20 missions were evaluated on a frame by frame basis totaling more than 40,000 frames of imagery. The processor properly recognized the M60A2 tank 90% of the time and improperly identified another vehicle as the M60A2 4% of the time. In all 20 missions the processor had established a good track on the target by 6000' and did not lose track for more than 0.5 seconds during the 90 second mission.

Captive Carry Flight Profile



CAPTIVE CARRY PROFILE

Figure 6.4-1. Captive Carry Test Flight Profile.

The captive carry flight profile which emulates the FOG-M missile profile is illustrated in Figure 6.4-1. The flight will initiate at a slant range of at least 7000' at an altitude of 850 ft. The processor is required to acquire and initiate a good track on the target by 5200'. At that point the pilot starts a descent onto the target at approximately a 9° depression angle. The pilot will continue to descend on the 9° approach angle in to at least 600' slant range. When reporting on the processor performance each flight pass over the target array is termed a mission. Several missions, including several headings and target array configurations, were flown to assess processor robustness and to gather a significant set of test results.

Test Area 3

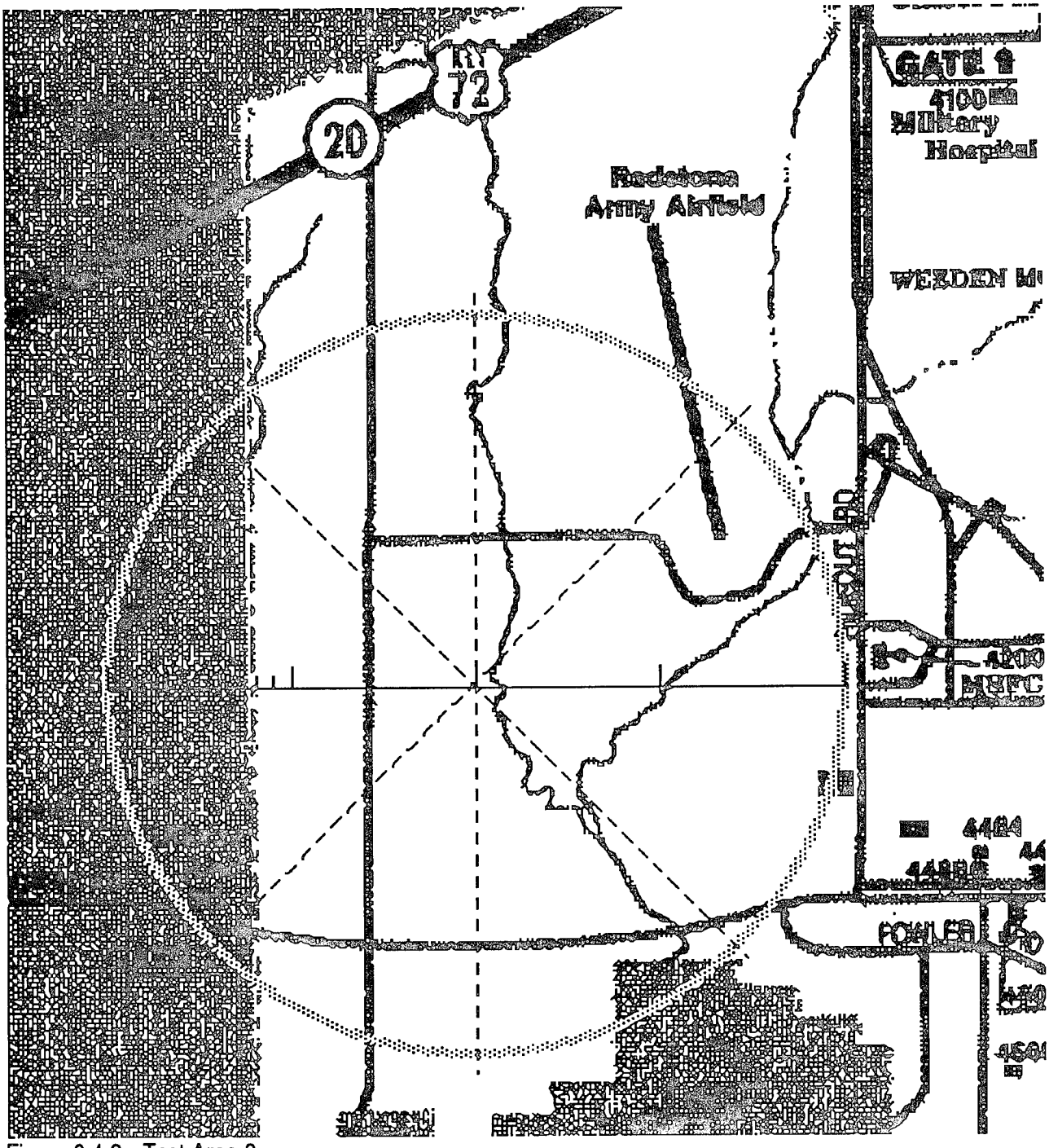


Figure 6.4-2. Test Area 3.

Figure 6.4-2 shows the approximate location of the target array on Test Area 3 (TA3). The target array will be positioned at the 2.5 km mark on TA3 as used in the previous captive carry imagery collections.

Captive Carry Testing

The target recognition task involves detecting, tracking and discriminating the M60A2 tank from an array of non-targets shown in Figure 6.3-4. The captive carry test is broken into two phases with the first phase evaluating the processor discrimination performance using the flight profile and basic target array as described.

The second phase included advance studies to test the robustness of the processor. To test the obscurration robustness of the processor the tank was backed about 20% into a tree line along the test area. Also a 55 gallon drum was added to the back end of the tank to alter its configuration. To add additional discrimination challenges to the processor a T-72 and second M60A2 tank were also added to the target array. To test the tracking robustness of the system several missions were flown while the tank was being driven in circles and other evasive maneuvers.

The processor starts each mission in search mode at approximately 7000' from the target area and is required to detect and establish a good track prior to the target leaving the bottom of the RSS field of view at approximately 5200'. The cursor overlay in search mode is a box with a dot in the center while the track mode is denoted by a plus (+) sign. Once in track mode the SPOTR will continue to track the M60A2 into a range of 650' or less. During the flight the sensor input to the processor is switched from an initial 2° field of view to an 8° at approximately 2000'. This is done to prevent the target from filling too large of a region of the field of view at closer ranges to the target. The net result is that the processor is presented with the same variation in target size twice during one flight pass. This doubles the number of opportunities to assess the processor performance and adds the ability to evaluate the differences created by two different sensors and fields of view.

Phase I Testing

Table 6.4-1. Captive Carry Phase I Test Sequence.

TEST	AZIMUTH	ELEVATION	HEADING	TARGETS	RANGE	LOCATION
Series 1 Test 1	240°	6°-12°	180°	CCII(ALL)	2K-200	TEST AREA 3
Series 1 Test 2	285°	6°-12°	225°	CCII(ALL)	2K-200	TEST AREA 3
Series 1 Test 3	330°	6°-12°	270°	CCII(ALL)	2K-200	TEST AREA 3
Series 1 Test 4	15°	6°-12°	315°	CCII(ALL)	2K-200	TEST AREA 3
Series 1 Test 5	60°	6°-12°	0°	CCII(ALL)	2K-200	TEST AREA 3
Series 1 Test 6	105°	6°-12°	45°	CCII(ALL)	2K-200	TEST AREA 3
Series 1 Test 7	150°	6°-12°	90°	CCII(ALL)	2K-200	TEST AREA 3
Series 1 Test 8	195°	6°-12°	135°	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 1	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 2	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 3	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 4	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 5	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 6	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 7	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3
Series 2 Test 8	RANDOM	6°-12°	RNDM	CCII(ALL)	2K-200	TEST AREA 3

During the first phase of captive carry testing missions were conducted using the basic test configuration described above. As seen in Table 6.4-1 the primary missions were flown as sets

of eight passes spaced at 45° increments. Other arbitrary headings were chosen to ensure generalization of the processors performance. Recordings were made of the 2° and 8° video inputs and the processor video overlay output in addition to storing the CRD text file of results in the laptop interfaced with the processor. During a mission the user interface was able to start the processor, make adjustments in the preprocessor gain, level and binarization threshold settings, make adjustments in the postprocessor threshold settings and to force the field of view switches. At the end of the mission the user would save the resulting text file to hard disk and reinitialize the processor for the next mission. The period for a mission was typically about 5 minutes with the data collection lasting approximately 90 seconds. The captive carry post test performance analysis was performed in the same manner as it was in the tower test.

The following is a description of the phase I sequence of tests.

Captive Carry Test Series 1

Test Range: Test Area 3
Sensor Height: 850'-20'
Target(M60A2) Motion: Stationary
Look Angle: <6° to >12°
Non Targets: A113, BMP, Pickup Truck 5t Rocket Launcher
Azimuth: 4-1 (240°, 285°,330°, 15°, 60°, 105°, 150°,195°), 4-2 (Random)
Filters Required: All TOPS, OTS
Test Criteria: Determine SPOTR performance compared to performance goals
Target Configuration: Barrel-10° up from horizontal, Turret-0°
VCR #1: WFOV RSS
VCR #2: NFOV RSS
VCR #3: SPOTR Output (CRV)

The following is the basic test procedures used in the captive carry testing.

1. Start conditions
   a. Pretest checkout complete, Target Position: TA3
   b. Target Look Azimuth: 240°
   c. Start Position: 0° Magnetic from Target Array, 850' AGL, 7000' Range
   d. Non Targets: All
   e. WFOV and NFOV
2. Perform OTS and determine that the processor is within baseline
3. Start VCR#1 VCR#2 and #3 in sync
4. Start the processor in search mode as the helicopter is crossing 7000' slant range approaching target array.
5. Monitor CRV as Helicopter completes the Captive Carry Profile to assure processor is correlating on the target and that the pass is successful.
6. Save text file of results to hard disk.
7. Proceed to new azimuth position for next test.

Phase II Testing

In phase II of the captive carry testing advanced studies were conducted to test the processor in ways not available previously while in the laboratory. The second phase included advance studies to test the robustness of the processor. To test the obscurration robustness of the

processor the tank was backed about 20% into a tree line along the test area. Also a 55 gallon drum was added to the back end of the tank to alter its configuration. To add additional discrimination challenges to the processor a T-72 and second M60A2 tank were also added to the target array. To test the tracking robustness of the system several missions were flown while the tank was being driven in circles and other evasive maneuvers. The same test procedures were applied as in phase I.

Captive Carry Test Results

The captive carry testing results exceed expectations. The preparations made in the tower testing provided a processor and test procedure which worked with minimal modification during the flight testing. The processor performed very well in both phases of the testing and exceeded our target recognition goals during many missions. On a frame-by-frame basis the processor maintained a 90% probability of recognition and a 4% false alarm rate for 20 missions or 40,000 frames of imagery. We were successful in acquiring the M60A2 tank at ranges out to 7800' and were able to maintain tracking into 600' while discriminating against other similar targets including a T-72 tank. At no time during the 20 missions did the processor lose track for more than 0.5 seconds and was always able to reestablish the proper track. The processor was able to acquire a M60A2 positioned 20% into a line of trees and also with a 55 gallon drum positioned on top of the chassis. The processor was able to maintain the proper track while descending onto the target while the turret of the tank was rotated through 360°. Finally, the processor was able to maintain the proper track while the tank was being driven in attacking and retreating maneuvers.

A minimum number of user interactions were required to maintain performance during a set of missions. In nearly 30 hours of operational flight testing over a period of four weeks the processor required minimal adjustments and no component replacements. Changing lighting conditions continued to cause variations in performance. Some of the sensitivity to lighting might be reduced by further algorithm efforts and the use of a gray scale input SLM, however it is believed that the dominant effect contributing to the lighting sensitivity is the use of a visible seeker and a lack of adjustment of its gain and level.

Table 6.4-2. Captive Carry Performance.

	Probability of Recognition (per frame)	False Alarm Rate (per frame)
Best Mission	94%	2%
Average Mission	80%	4%
8° FOV Mission	90%	4%
2° FOV Mission	71%	4%

A captive carry mission is defined as a single helicopter flight over the target from 6500' into 600'. These missions include instances of static and dynamic targets as well as several non target vehicles and background clutter. Over one hundred missions were flown over the four weeks of captive carry testing in which the processor properly acquired and tracked the M60A2. Twenty missions were selected for post test analysis. The criteria for selecting these missions included an equal sampling of missions from Phase I and II, complete coverage of all the azimuth headings flown, a sampling of missions over the course of the four week test period, and during the mission the processor must have successfully acquired the target in the search space of the flight profile. The 20 missions analyzed result in over 40,000 frames of captive carry imagery which was processed at 15 frames/sec. The processor performance is summarized in Table 6.4-2. On each of the 20 missions analyzed the processor engaged the target in track mode by 5500 feet with a 2° FOV sensor. Once in track mode the processor did not lose track into a range of 600 feet for more than 0.5 seconds over a period of approximately 90 seconds.

The processor was successful in acquiring the target at all of the azimuths presented to it during the phase I testing. There was a general trend that the processor would perform better for those instances in which the target was broadside relative to the seeker however successful missions were conducted from the end-on positions as well. The processor was successful in acquiring the target anywhere in the search space defined from 7000' to 5200'. There was an observed trend between the orientation of the target and the typical acquisition range of that target. Acquisition was more probable at the 7000' range for broadside target orientations and was typically at about 6000' for end-on target orientations. This follows the trend defined by the Johnson criteria for target recognition as related to the number of pixels on target and the probability of recognition. During phase I testing we intentionally flew some missions in which the flight profile was violated in elevation (depression) angle. The processor was robust up to the 16° elevation angle presented to it in the worst case mission. This is a 4° departure from the angles represented in our filter data base.

In the phase II testing several studies were made to present more challenging target recognition tasks to the processor. These challenges included the inclusion of a second tank of the same and different type in the target array, articulation of the target turret and gun barrel, the addition of a 55 gallon drum to the target, parking the target in a line of trees and driving the target to introduce azimuth change in addition to the range to target change.

The processor performed as expected with the addition of a second M60A2 into the target field of view. First the second target was oriented identical to the first such that the same filter should correlate well on both. Two missions were flown and in both cases the highest correlation response oscillated between the two tanks. The correlation response of the two tanks differed by only a few percent and would vary as a function of where the targets occurred in the field of

view. When one of the targets is rotated in azimuth relative to the other the one with the more broadside aspect responded with a stronger signal and was the more likely to be tracked.

The processor performed very well in discriminating the M60A2 from the T-72 Soviet tank. This study was conducted to determine the ability of the processor to perform simple identification of friend or foe functions. The processor was successful in identifying the M60A2 as a friendly with probabilities above 95% for several missions flown. The tanks were oriented at different azimuths and the missions were flown from various headings such that from mission to mission the tank with the more broadside orientation changed from the M60A2 to the T-72. In all of the testing conducted the processor never lost track of the M60A2. The processor performance was slightly poorer for the end-on M60A2 however no track was ever initiated on the T-72.

Several tests were conducted to assess the sensitivity of the processor to target articulation. The turret of the target was rotated through 360° while flying two missions. In both missions the orientation of the turret relative to the tank had no effect on the ability to maintain track. The processor performance was slightly poorer at closer ranges where the orientation of the turret was more resolved and was different from that of the filter reference. Similar results were found when the gun barrel was raised and lowered. A third set of tests involved adding a 55 gallon drum to the back end of the tank chassis representing a different target configuration. Several missions were flown while the target was in this condition with no effect on the ability to acquire and track the target even at the closest ranges.

Additional clutter and target obscurration was introduced by backing the M60A2 tank about 20% into a line of trees. Several missions were flown at the target from the hemisphere of azimuths on the open side of the tree line. The processor was able to acquire and track the target from all azimuths. These tests were the most difficult for the processor and would not be well represented by the results in Table 6.4-2. There are two primary explanations for the poorer performance which included the preprocessor algorithm and the unfavorable lighting conditions. Placing the target against the tree line represents a poor target to background contrast situation. Also there are several variations in lighting levels between the trees, their shadows and the sun light breaking through between the trees. Based on the preprocessing algorithm used many of the available "on" pixels in the binary image were allocated to these lighting variations in the trees instead of defining the tank. This in conjunction with the poor lighting conditions on the day of the test contribute to the poorer processor performance during this testing.

Finally, several tests were conducted in which the target was driven while the mission was being flown. This represents the complete test of the filter manager in that azimuth, range and elevation are changing simultaneously but at possibly different rates during the mission. These tests included driving the target in a circle, driving the tank in a series of "S" turns in an attacking manner toward the oncoming seeker, and in a retreating manner away from the oncoming seeker. The results for all three tests were similar. The processor was able to acquire and track the target in all three situations. However, the processor performance was better when the target was more broadside than end-on.

The captive carry tests were conducted over two hour periods during a window from 0900 to 1500 hours during the four weeks of August. In general the time of day had an effect on which azimuth headings would result in the best mission performance. The conditions which resulted in back lighting of the target array relative to the seeker provided the best target recognition situation. These conditions seemed to be more important to recognition performance than the

target orientation relative to the seeker (pixels on target) or the articulation of the target. This is consistent with the fact that the filters were developed from reference images which provided very strong silhouettes when binarized similar to that from backlit targets in the captive carry imagery.

In summary, the processor and pattern recognition algorithms performed very well. We were able to acquire and track the target with high confidence from a variety of azimuth headings and ranges to target. This performance was maintained while the target was articulated and driven in an elusive manner. The processor was able to maintain excellent discrimination with a variety of other military targets present and demonstrated an ability to support a passive identify friend-or-foe function. Finally the processor was able to acquire and track an obscured target in a lower contrast situation with slightly lesser performance. However our processing performance has been demonstrated to be effected by the number of pixels on target and the amount of target to background contrast.

Processor Robustness and Reliability

During the eight weeks of testing including four weeks in captive carry testing the processor did not need any significant component replacements or adjustments. There were no optical subsystem failures recorded during that period. Twice during the testing we made adjustments to the half wave plates in the optical subsystem to optimize optical throughput. This is believed to be necessary when the temperature changes considerably as when going from the tower laboratory to the open-air helicopter. When this happens the amount of polarization rotation modulated by the SLM changes and thus the wave plate adjustment is required. This was anticipated and designed into the mechanical architecture which makes this adjustment relatively fast and easy.

During operation there were a few instances in which the processor would electronically fail in operation. There are two known causes for these failures which would either require the reinitialization of the mission software or necessitate the rebooting of the CPU. The first failure is in the postprocessor. If a sufficient number of correlation responses were determined to be above a defined threshold value the postprocessor readout would encounter a limitation which would cease the generation of the detection interrupt. This would result in the CPU never detecting the interrupt and thus never commanding the preprocessor to overlay the cursor on the output video. This problem could be corrected by reinitializing the mission software and adjusting upward the postprocessor threshold. The second failure was a result of the preprocessor. This failure is inherent in the design of the commercial off the shelf GPB-1 image processing board. The failure would manifest itself if too many adjustments were made in the binarization level or in the A/D gain and level adjustments during a mission. This failure would "lock up" the system. The processor must be restarted to recover from this failure.

Demonstration Day Attendance

As during the tower testing, three days of captive carry testing were dedicated for onsite visitation from interested parties. The captive carry demonstration was very well attended and received. Several attendees were on hand from various MICOM offices as well as many invited guests from around the country. The processor performed very well on the first and third days of the demonstration. The atmospheric visibility was extremely poor due to high humidity on the second day and resulted in intermittent processor performance.

7.0 Other Activities

In addition to the development of the algorithms, hardware, and pattern recognition testing; various other activities have been conducted in support of the TOPS program over the three year period of performance.

Papers and Presentations

• Wrote and presented two papers at the April, 1992 SPIE Conference in Orlando. The first paper was a general program overview and the second focused on the filter formulations and distortion sensitivity analyses.

• Wrote and presented three papers at the April 1993 SPIE conference in Orlando. The three topics included a program overview, a discussion of preprocessing, and a discussion of correlation filtering, postprocessing and the development of the SPOTR emulator.

• Wrote and presented a paper at the April, 1994 SPIE Conference in Orlando. The paper was a general program overview. The paper gave program status and a video tape of the Flyable Prototype in operation while under vibration environments was shown.

• Wrote an article which was published in the May 1994 SPIE International Working Group for Optical Computing and Processing Newsletter.

• Writing and presenting two papers which summarize the TOPS program at the Orlando April, 1995 SPIE Conference. The first paper will describe the ATR algorithms and their implementation to video and FLIR imagery. The second paper will provide a program overview and highlight the recent field test results.

Transfer of Technology Activities

We have been very successful in the transfer of the optical pattern recognition technology into other services and program offices. Several pattern recognition programs have resulted from the efforts and support TOPS. We have completed a successful program with the Naval Surface Warfare Center in detecting periscopes in FLIR imagery. We have recently completed a very successful program with the US Navy SPAWAR in performing acoustic signature processing for anti-submarine activities. There are two ongoing programs which resulted from the efforts of the TOPS program. We are currently supporting US Army MICOM in the development of a proof feasibility demonstration using the SPOTR to process FLIR imagery. A second program with the USAF Wright Laboratories at Eglin AFB will integrate a processor very similar to the SPOTR with a LADAR in a remotely piloted vehicle. Several other interfaces have been established including the Army, ARPA, the Air Force and the Navy. In addition, we are working to integrate aspects of the TOPS technology into an X-ray processing system to support mammogram analysis.

Technical Meeting Support

We attended the kickoff of a consortium of electro-optical component providers and users hosted and organized by Andy Yang.

We conducted several status briefings to Joe Horner, Richard Juday, Bill Friday, and Brian Hendrickson during the last three years.

We participated in the 10th and 11th Annual ARPA Optics Reviews.

We supported the Texas Instruments & ARPA Deformable Mirror Device (DMD) direction meeting and have provided many follow up suggestions for the development of the phase-only DMD.

Imagery and Data Provided

- We provided an input to Andy Yang which projected the current and near future capabilities of optical and electronic pattern recognition.

- We have delivered selected Captive Carry II and turntable imagery to Joe Horner, Richard Juday, Dennis Goldstein and Richard Simms.

- We have developed several video tapes which describe the TOPS program and its field testing successes.

- We have delivered various TOPS viewgraphs and photographs to a variety of interested requestors.

8.0 Engineers Contributing to Research

University of Dayton Research Institute

Dave Flannery

Bolder Nonlinear System

Roylynn Serati
Steve Serati
Gary Sharp

Martin Marietta

Kipp Bauchert
Woody Brison
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John Campolong
Paul Cogeos
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Jack Eastman
Mike Gildner
Roger Green
Bill Hahn
Mike Henry
Dave Homan
Ed Knowles
Scott Lindell
Wade Loustalet
Jim Lundgren
Tom Richards
Jeff Robb
Phil Roberts
Gary Shapiro
Wayne Simon
Greg Starkey
Neil Tice
Andy Tomko
Tim Welden

9.0 Summary

The Martin Marietta TOPS Optical Pattern Recognition program was very successful. The program met or exceeded all technical objectives. The processor correlates at greater than 800 Hz, has an input frame rate of 15 Hz, conducted the captive carry flight testing with greater than 90% probability of recognition and less than a 4% false alarm rate. The system occupies less than 1 ft^3, weighs less than 44 lbs and consumes less than 76 Watts of power. The technical objectives were accomplished within one week of the scheduled 36 months and were conducted at cost.

A secondary objective of the TOPS program is to find users for the optical processing technology. The Martin Marietta TOPS Optical Pattern Recognition program has been carried forward to the U. S. Army TACAWS missile project. The optical processor is being considered for use as part of the guidance and control system for the tactical weapon system. Other projects which have been made possible by the TOPS program include a successful periscope detection program with the Naval Surface Warfare Center, a successful acoustic processing Advanced Technology Demonstration program with US Navy SPAWAR, and a recent award of a program to use the same processor design integrated with a laser radar sensor in a remotely piloted vehicle for the USAF Wright Laboratories at Eglin AFB. Several other programs are in the discussion phase at this time.

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